

Round Rock 13.3" Schematics Document

Haswell ULT

2013-06-28
REV : SSI

DY : None Installed
XDP: For CPU XDP Debug Port installed
PCH_XDP: For PCH XDP Debug Port installed

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

Round Rock 13.3" UMA

Rev
X00

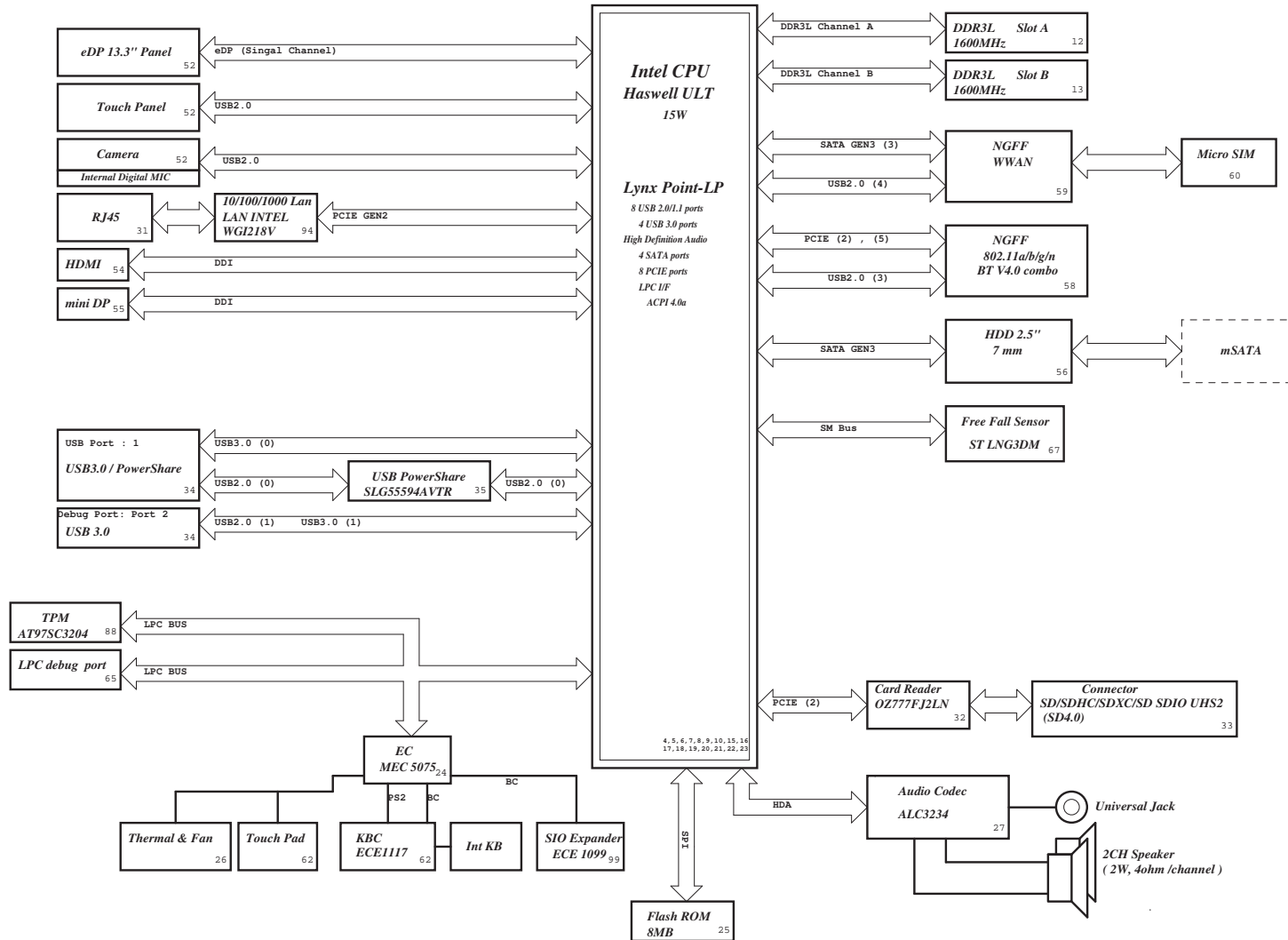
Date: Friday, June 28, 2013

Sheet 1 of 107

Round Rock 13.3" Block Diagram

Project code : 91.40A01.001
PCB P/N : 13229
Revision : X00

CHARGER BQ24715 44	
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC TPS51275 45	
INPUTS	OUTPUTS
DCRATOUT	3.3V_AUX_S5 3.3V_S5 5V_S5
CPU DC/DC TPS51622 46~47	
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE
SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCRATOUT	ID05V_M
SYSTEM DC/DC TPS51363 & APL5338 49	
INPUTS	OUTPUTS
DCRATOUT	ID05V_S3 ID0675V_S0 DDR_VREF_S3
Load Switches 36	
INPUTS	OUTPUTS
5V_S3 3.3V_S3	5V_S0 3.3V_S0 3.3V_S5_PCH 3.3V_M 3.3V_LAN ID05V_MODPHY ID05V_S0
PCB LAYER(FR4-6 Layer)	
L1:Top	L6:Bottom
L2:PW/GND	
L3:Signal	
L4:Signal	
L5:PW/GND	



5

4

3

2

1

D

C

B

A

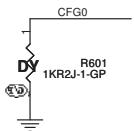
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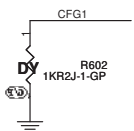
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>CPU (PCIE/DMI/FDI)</i>			
Size A4	Document Number		Rev
	<i>Round Rock 13.3" UMA</i>		<i>X00</i>
Date: Friday, June 28, 2013	Sheet	3 of	107

SSID = CPU

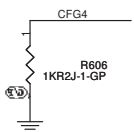
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	0: Lane Reversed 1: (Default) Normal Operation; No stall



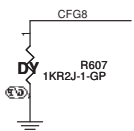
PCH/PCH LESS MODE SELECTION	
CFG1	0: Lane Reversed 1: (Default) Normal Operation



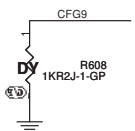
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



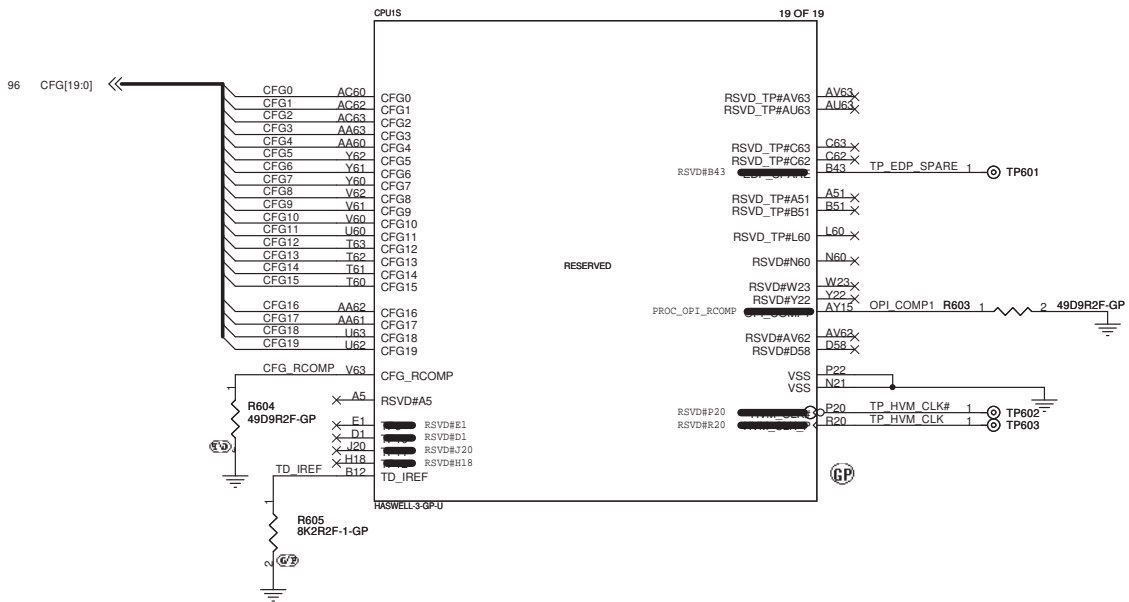
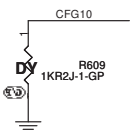
ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegrardless of the locking of the unit



NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0: No VR support SVID is present The chip will not generate(OR Respond to) SVID activity



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED



<Core Design>

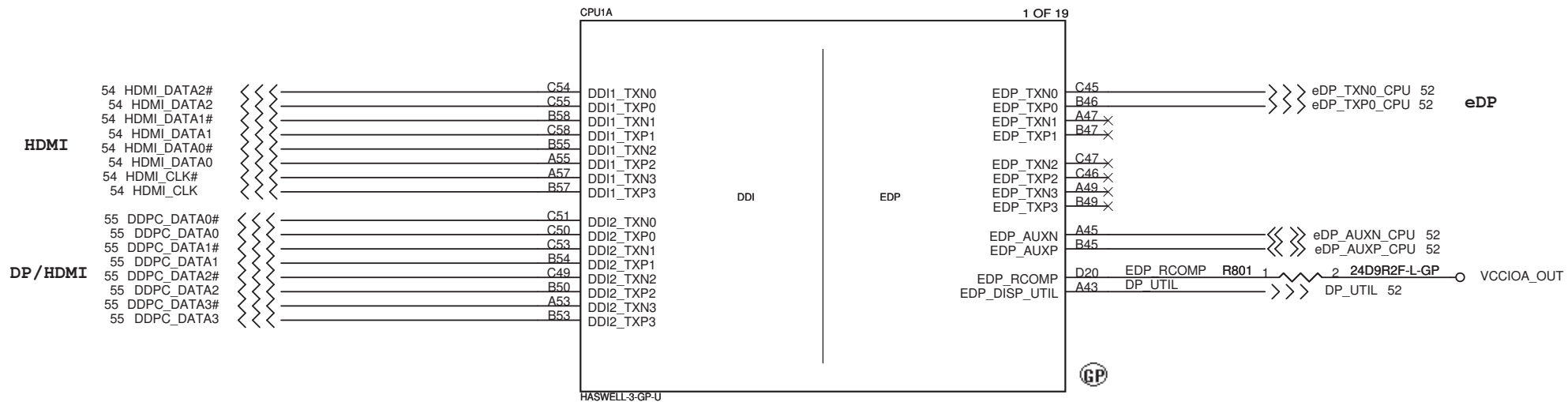
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (RESERVED)**

Size A3 Document Number: **Round Rock 13.3" UMA** Rev **X00**

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SSID = CPU



<Core Design>



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Title

CPU (DDI/EDP)

Size
A4

Document Number

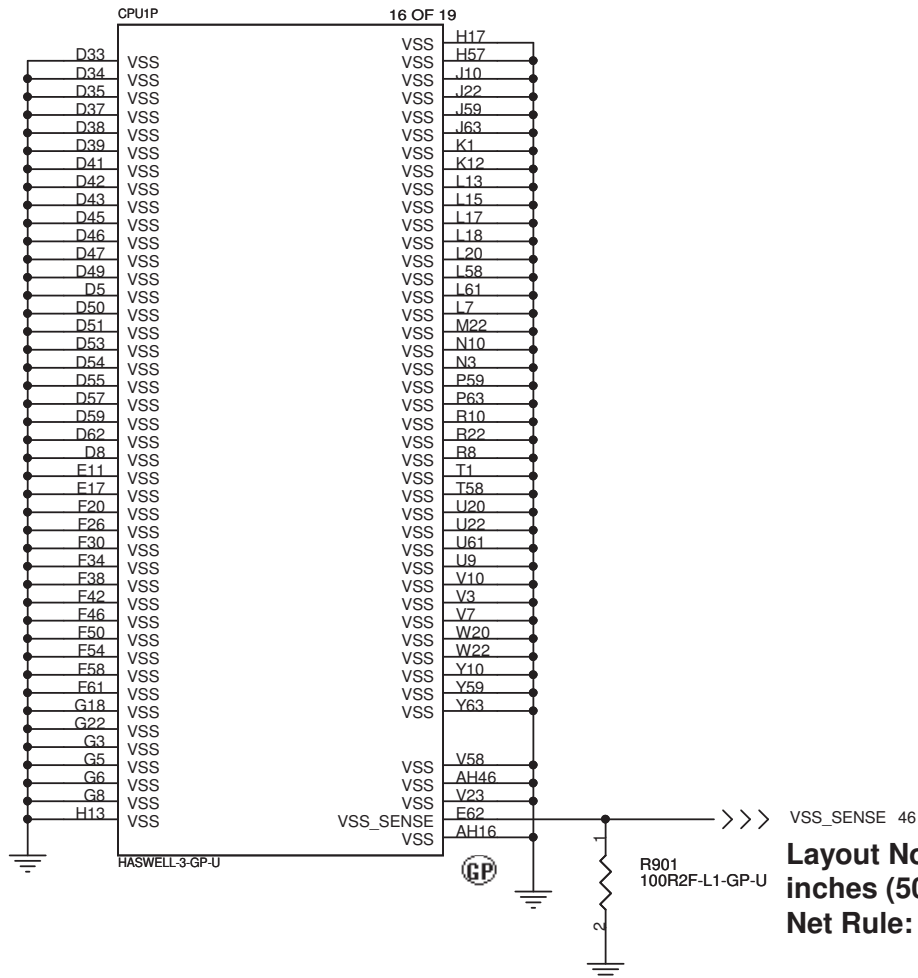
Round Rock 13.3" UMA

Rev
X00

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SSID = CPU



Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.
Net Rule: VCC_SENSE and VSS_SENSE differential signals

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Title

CPU (VSS)

Size
A4

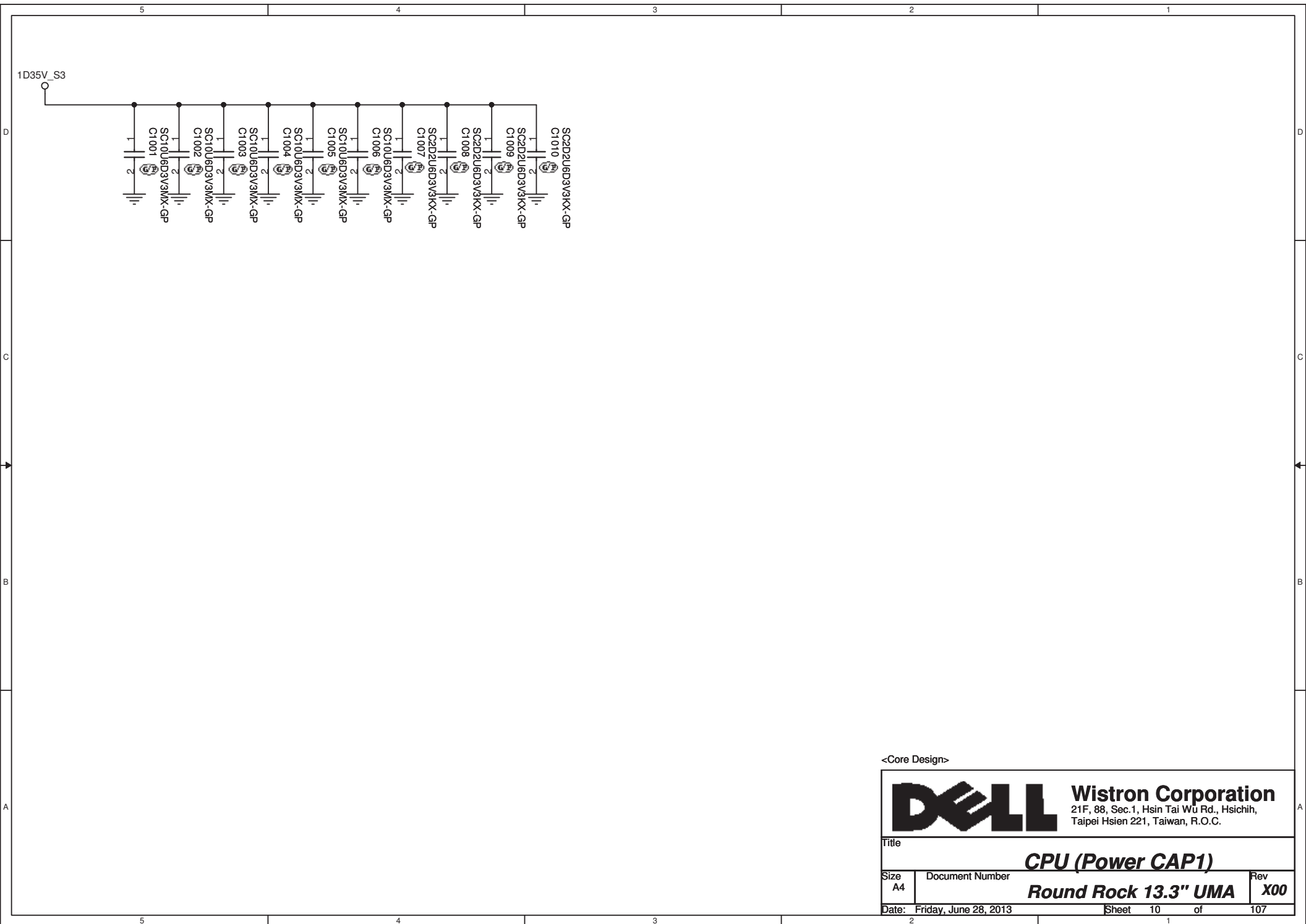
Document Number

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X00

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<Core Design>

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Title			
CPU (Power CAP1)			
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Title

CPU (Power CAP2)

Size
A

Document Number

Round Rock 13.3" UMA

Rev

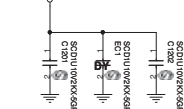
X00

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Layout Note:

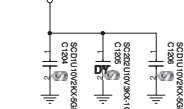
Place these caps close to VREF_CA

M_VREF_CA_DIMMA
Ω

Layout Note:

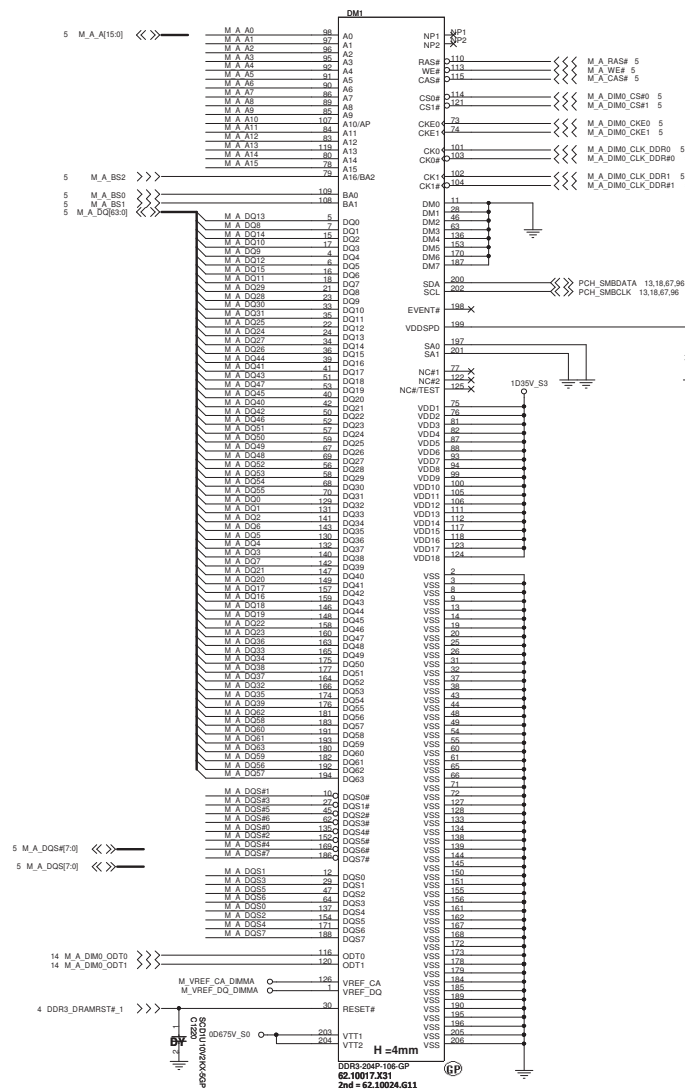
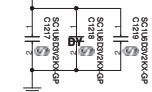
Place these caps close to VREF_DQ

M_VREF_DQ_DIMMA



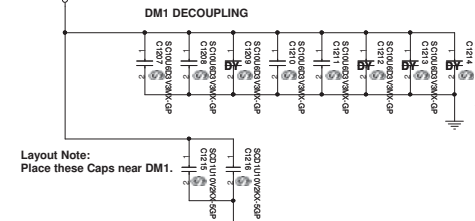
0D675V_S0

Place these caps
close to VTT1 and VTT2.



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



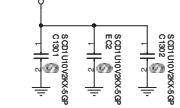
Layout Note:
Place these Caps near DM1

&ltCore Design>

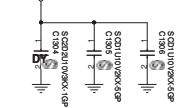


SSID = MEMORY

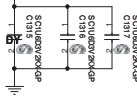
Layout Note:
Place these caps close to VREF_CA
M_VREF_CA_DIMMB



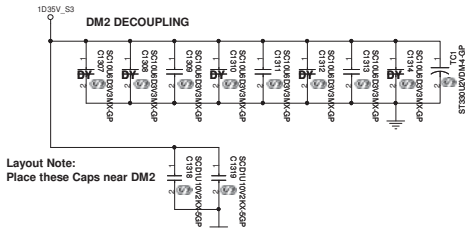
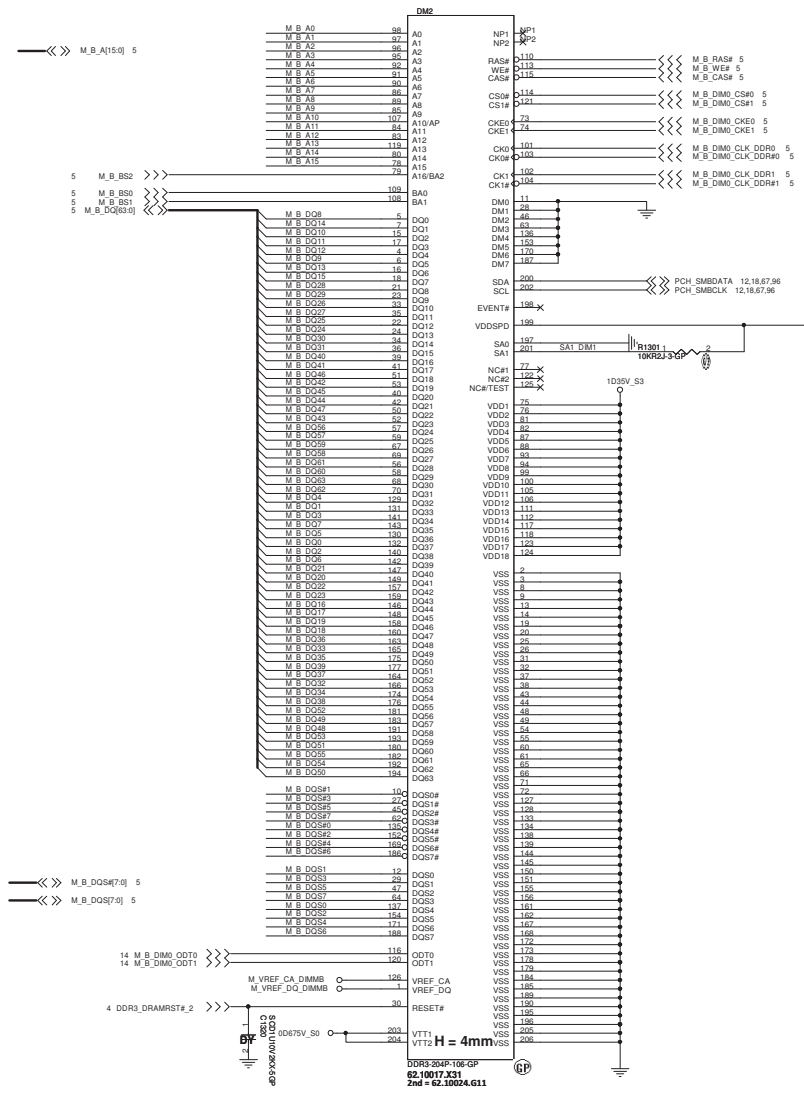
Layout Note:
Place these caps close to VREF_DQ
M_VREF_DQ_DIMMB



Place these caps
close to VTT1 and VTT2.



DQS1	DQ0	M_B_DQ8
	DQ1	M_B_DQ14
	DQ2	M_B_DQ10
	DQ3	M_B_DQ11
	DQ4	M_B_DQ12
	DQ5	M_B_DQ9
	DQ6	M_B_DQ13
DQS3	DQ8	M_B_DQ28
	DQ9	M_B_DQ29
	DQ10	M_B_DQ26
	DQ11	M_B_DQ27
	DQ12	M_B_DQ25
	DQ13	M_B_DQ24
	DQ14	M_B_DQ30
DQS5	DQ16	M_A_DQ40
	DQ17	M_A_DQ41
	DQ18	M_A_DQ46
	DQ19	M_A_DQ42
	DQ20	M_A_DQ45
	DQ21	M_A_DQ44
	DQ22	M_A_DQ47
DQS7	DQ24	M_A_DQ56
	DQ25	M_A_DQ57
	DQ26	M_A_DQ59
	DQ27	M_A_DQ58
	DQ28	M_A_DQ61
	DQ29	M_A_DQ60
	DQ30	M_A_DQ63
DQS8	DQ31	M_A_DQ62
	DQ32	M_A_DQ4
DQS0	DQ33	M_A_DQ1
	DQ34	M_A_DQ3
	DQ35	M_A_DQ7
	DQ36	M_A_DQ5
	DQ37	M_A_DQ0
	DQ38	M_A_DQ2
	DQ39	M_A_DQ6
DQS2	DQ40	M_A_DQ21
	DQ41	M_A_DQ20
	DQ42	M_A_DQ22
	DQ43	M_A_DQ23
	DQ44	M_A_DQ16
	DQ45	M_A_DQ17
	DQ46	M_A_DQ19
DQS4	DQ47	M_A_DQ18
	DQ48	M_A_DQ36
	DQ49	M_A_DQ33
	DQ50	M_A_DQ35
	DQ51	M_A_DQ37
	DQ52	M_A_DQ39
	DQ53	M_A_DQ32
DQS6	DQ54	M_A_DQ34
	DQ55	M_A_DQ38
	DQ56	M_A_DQ52
	DQ57	M_A_DQ49
	DQ58	M_A_DQ48
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	DQ62	M_A_DQ54
	DQ63	M_A_DQ50

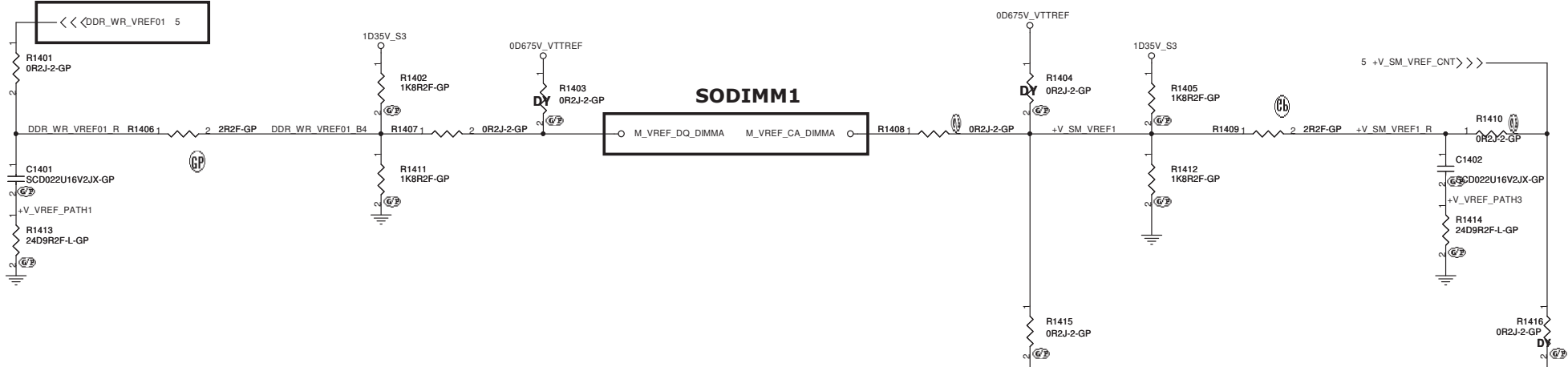


Layout Note:
Place these Caps near DM2

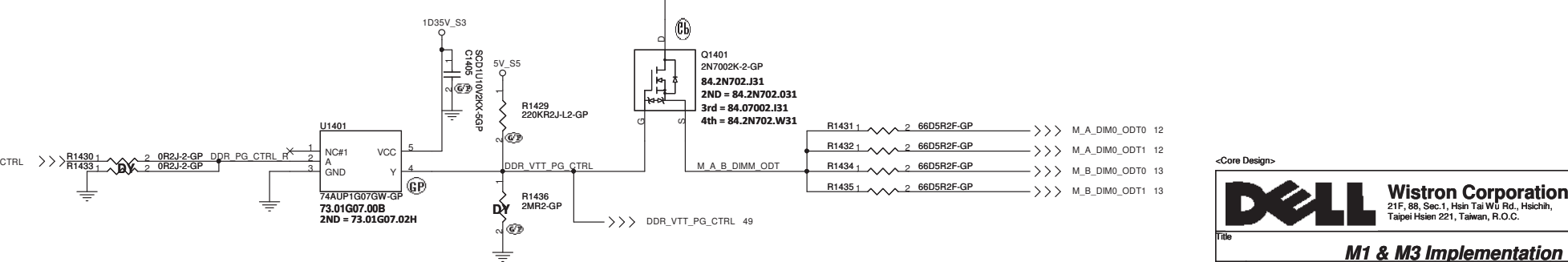
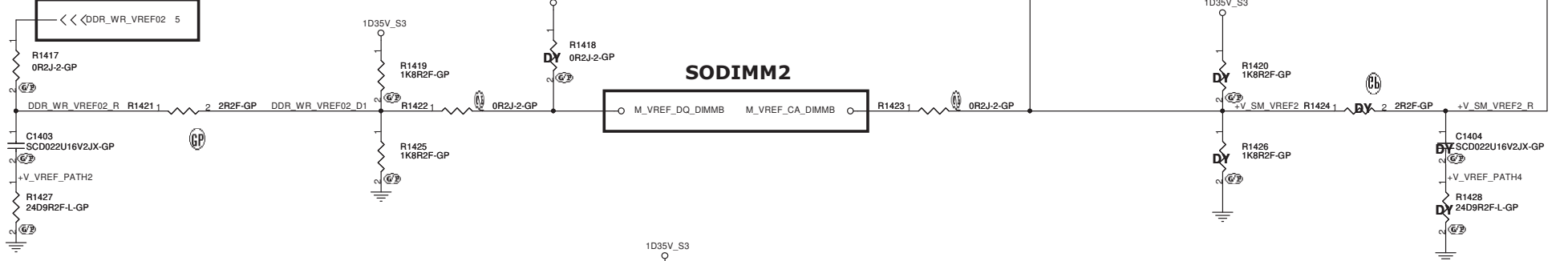
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from
the Processor than SO-DIMMA

SSID = MEMORY VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

SA_DIMM_VREFDQ
Driven by process (PIN#AR51)



SB_DIMM_VREFDQ
Driven by process (PIN#AP51)



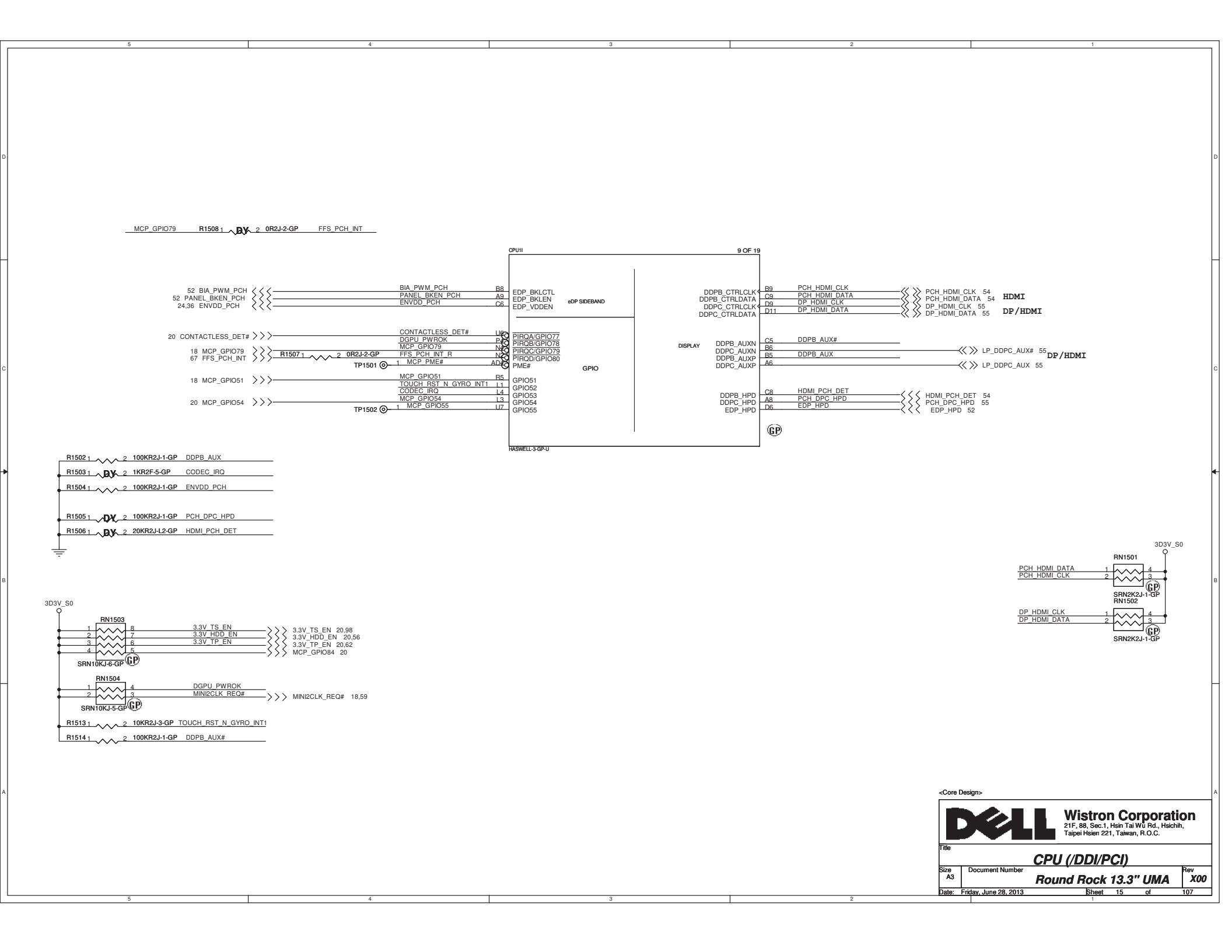
<Core Design>

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Title: **M1 & M3 Implementation**

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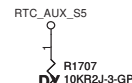
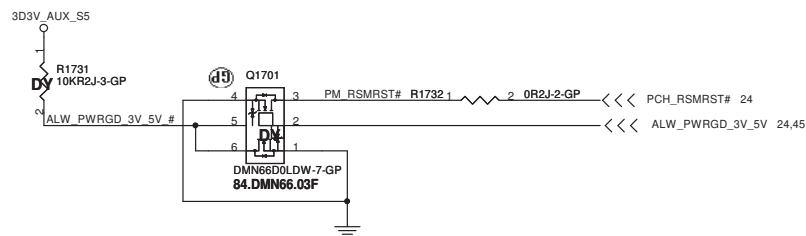
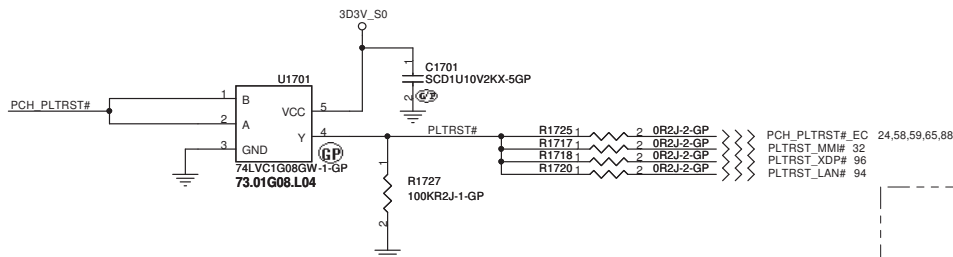
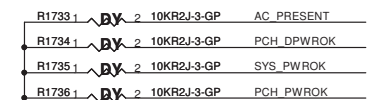
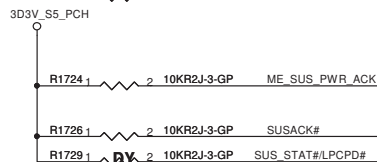
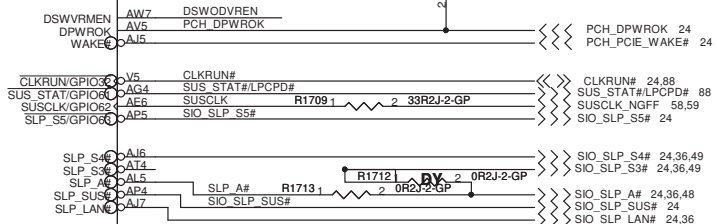
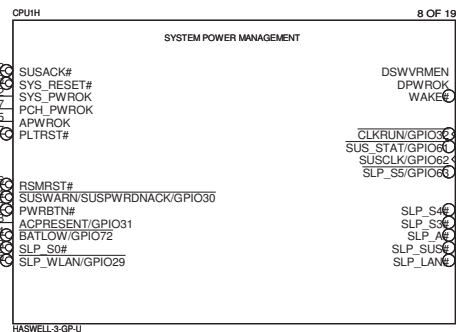
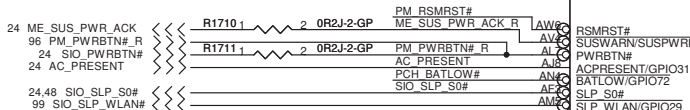
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<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU (DDI/PCI)			
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NOTE:
PWRBTN# Integrated Pull-Up.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

DSWODVREN

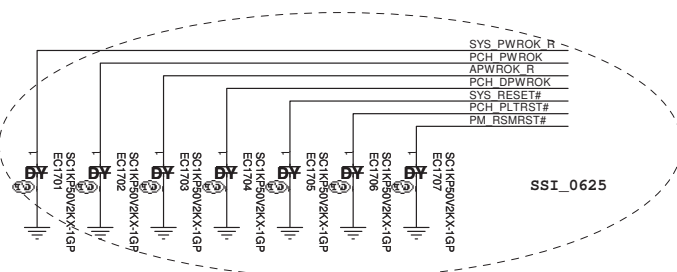
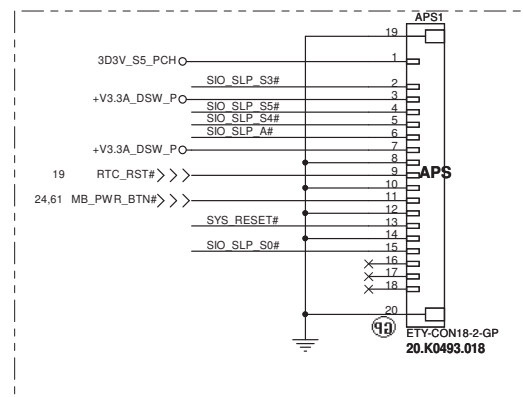
R1721 1

R1723 1

R1720 330KR2J-L1-GP

RTC_AUX_S

D



21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Round Rock 13.3" UMA

Size

Document Number

Rev

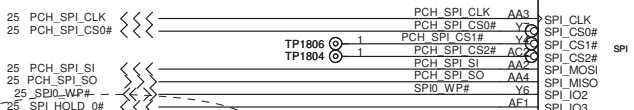
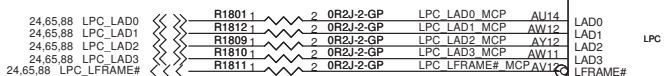
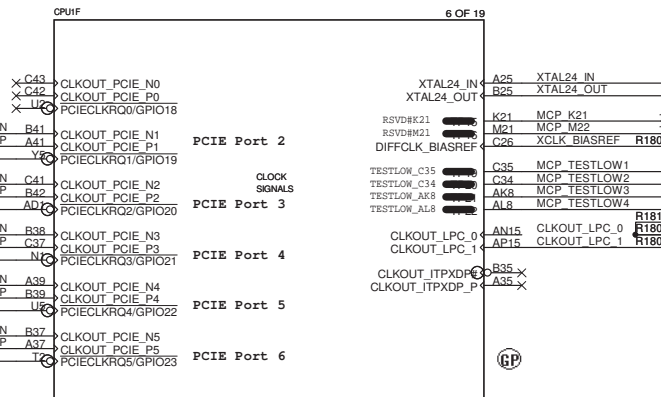
Date: Friday, June 28, 2013

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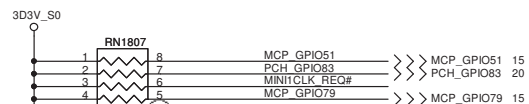
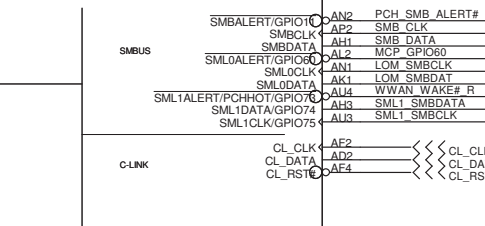
Date _____

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

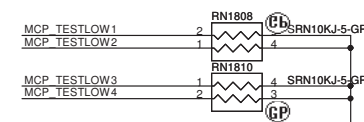
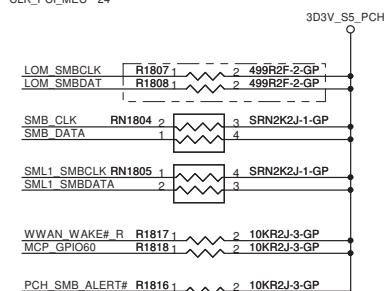
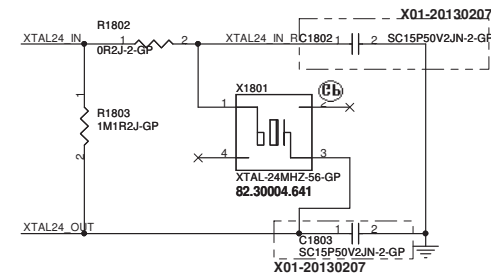
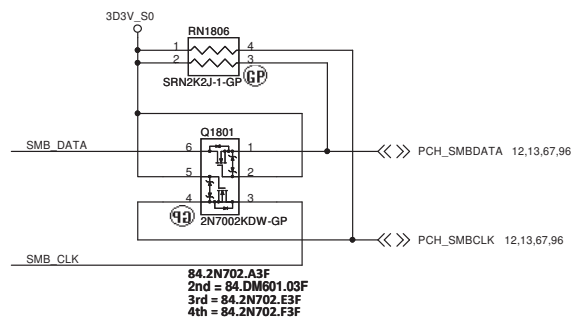
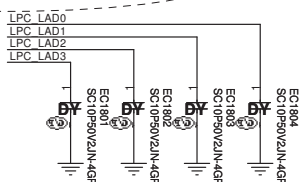
32 CLK_PCIE_CARD#	32 CLK_PCIE_CARD	20.32 MINICLK_REQ#	94 CLK_PCIE_LAN#	94 CLK_PCIE_LAN	20.94 LANCLK_REQ#	58 CLK_PCIE_N3_WLAN#	58 CLK_PCIE_P3_WLAN	58 MINICLK_REQ#	58 CLK_PCIE_N4_WLAN#	58 CLK_PCIE_P4_WLAN	58 MINICLK_REQ#	58 CLK_PCIE_N5_WWAN#	58 CLK_PCIE_P5_WWAN	15.58 MINICLK_REQ#
<p>PCIE Port 2</p> <p>PCIE Port 3</p> <p>PCIE Port 4</p> <p>PCIE Port 5</p> <p>PCIE Port 6</p>														



SSSI 0618



SSSI 0625



<Core Design>



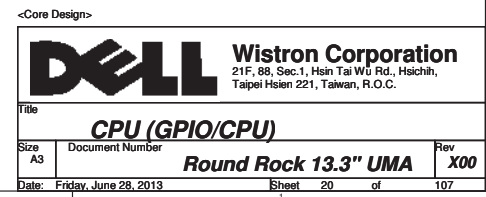
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

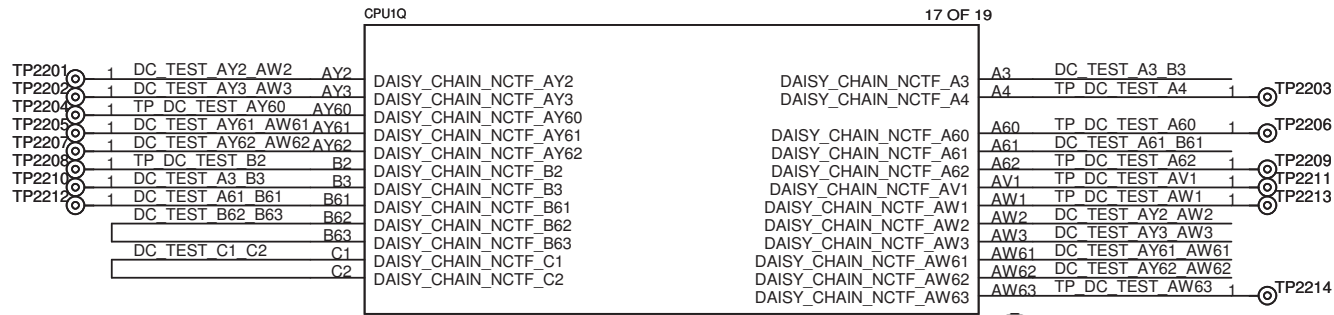
CPU (CLOCK/SMBUS/CL/LPC/SPI)

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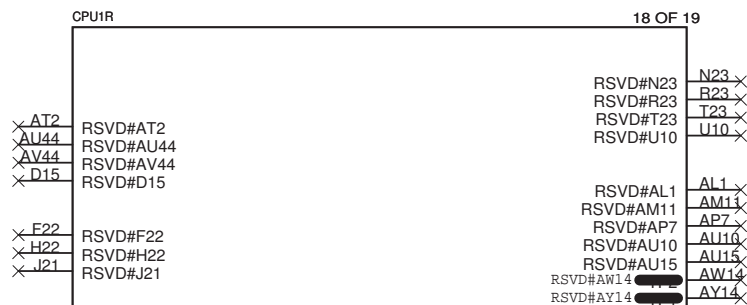
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WWW.AliSaler.Com





HASWELL-3-GP-U



HASWELL-3-GP-U



<Core Design>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size
A4

Document Number

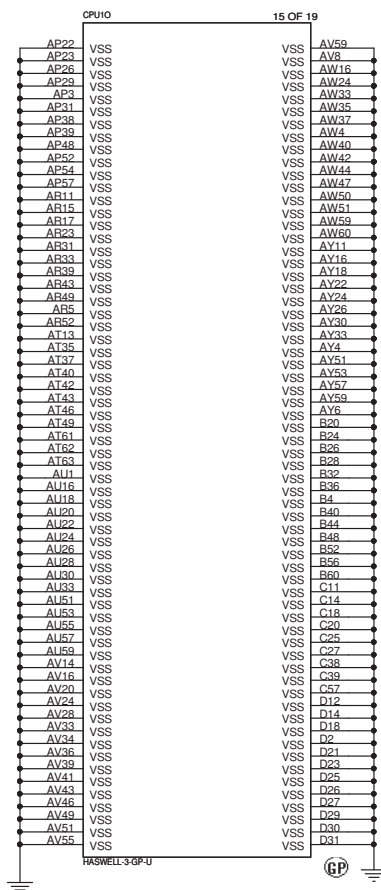
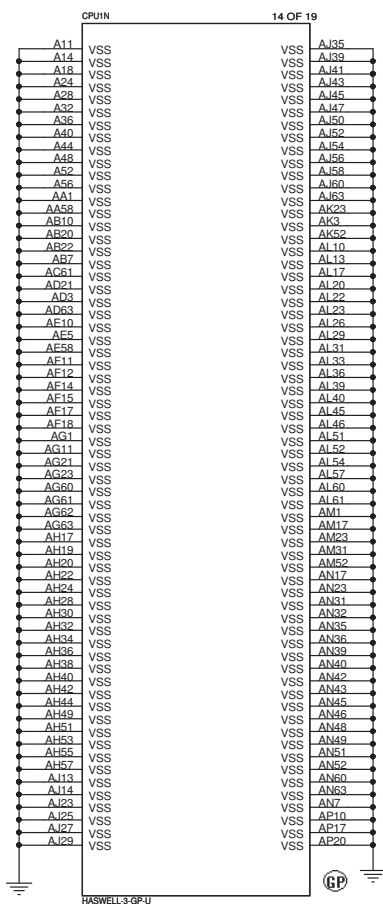
Round Rock 13.3" UMA

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X00

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SSID = PCH

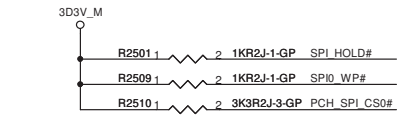


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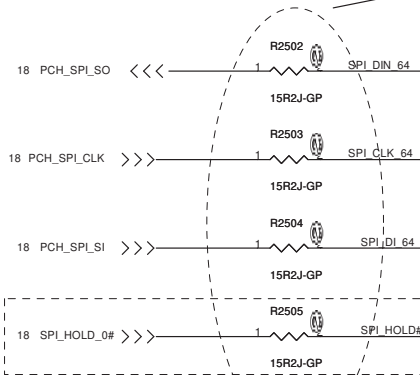
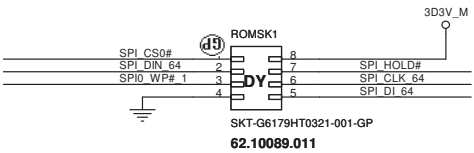
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Title CPU (VSS)				
Size A3	Document Number Round Rock 13.3" UMA			Rev X00
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SSID = Flash.ROM

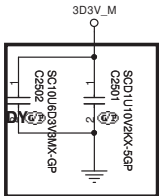
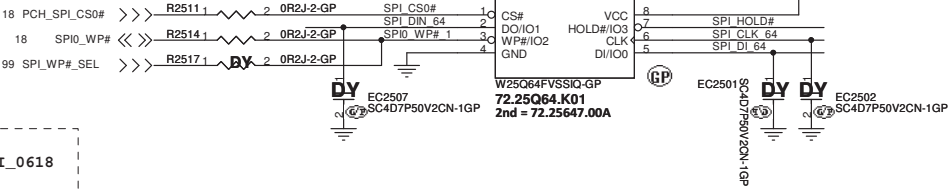
SPI ROM Equal length need to less than 500mil



Schematic Design Checklist
Single Device: 15
Multiple Devices: 33 per branch

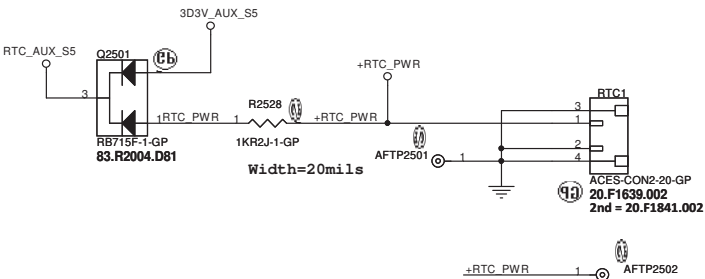


SYSTEM SPI ROM
SPI Flash ROM(8M) for PCH



Layout Note: Close to U2501 Pin 8

SSID = RTC



<Core Design>

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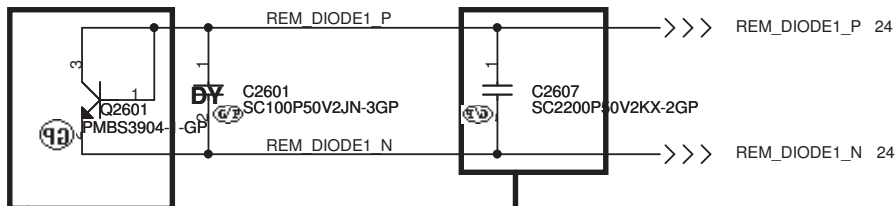
Title: **Flash/RTC**

Size: A3 Document Number: **Round Rock 13.3" UMAX00** Rev

Date: Friday, June 28, 2013 Sheet 25 of 107

SSID = Thermal

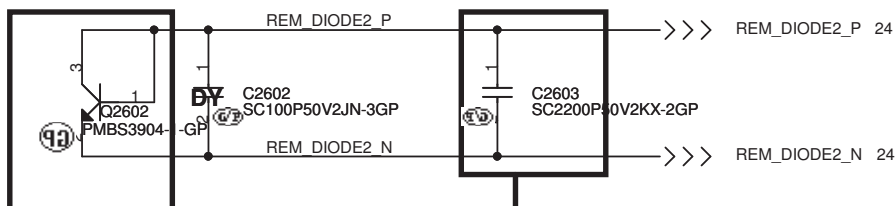
84.03904.L06
2ND = 84.03904.P11



Layout Note: Place to CPU

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

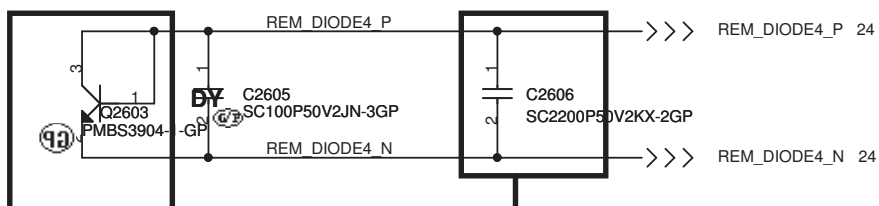
84.03904.L06
2ND = 84.03904.P11



Layout Note: Place to DIMM

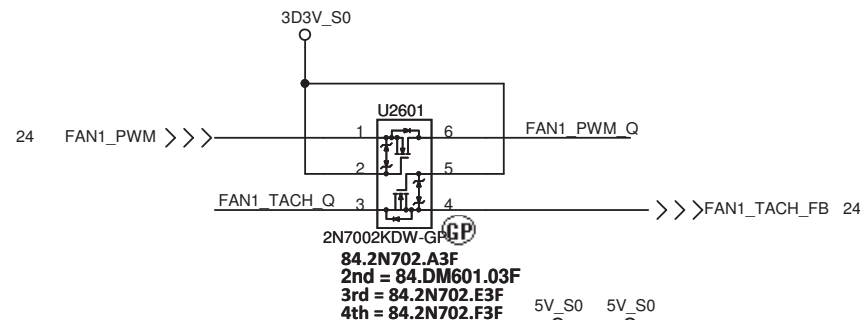
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

84.03904.L06
2ND = 84.03904.P11



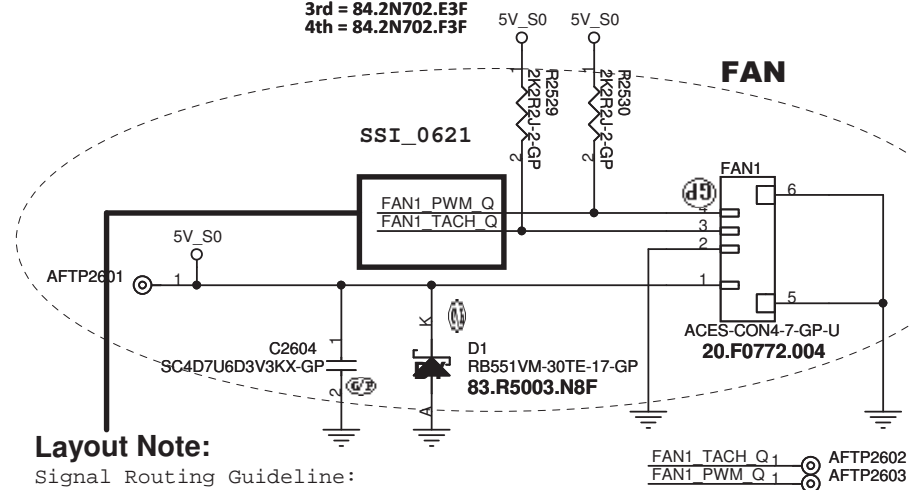
Layout Note: Place to V.R

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



Layout Note:

Signal Routing Guideline:
Trace width = 15mil



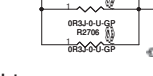
<Core Design>



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Title Thermal/Fan		
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SSID = AUDIO



Place close to Pin 26



```

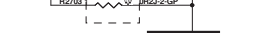
trace width=30mil
p2210 p2211 near GDR

```

Digital



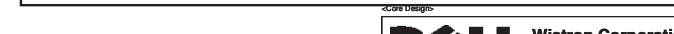
10



	Analog
Digital	



SA SPKR



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<Core Design>



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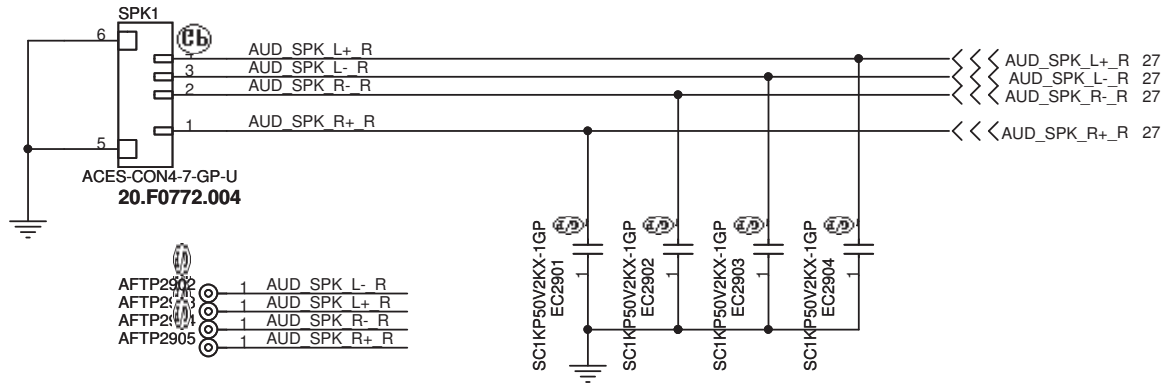
Date: Friday, June 28, 2013

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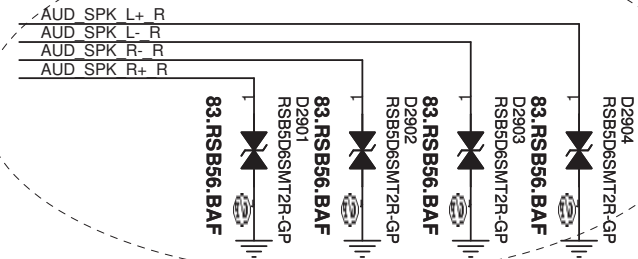
SSID = AUDIO

Speaker

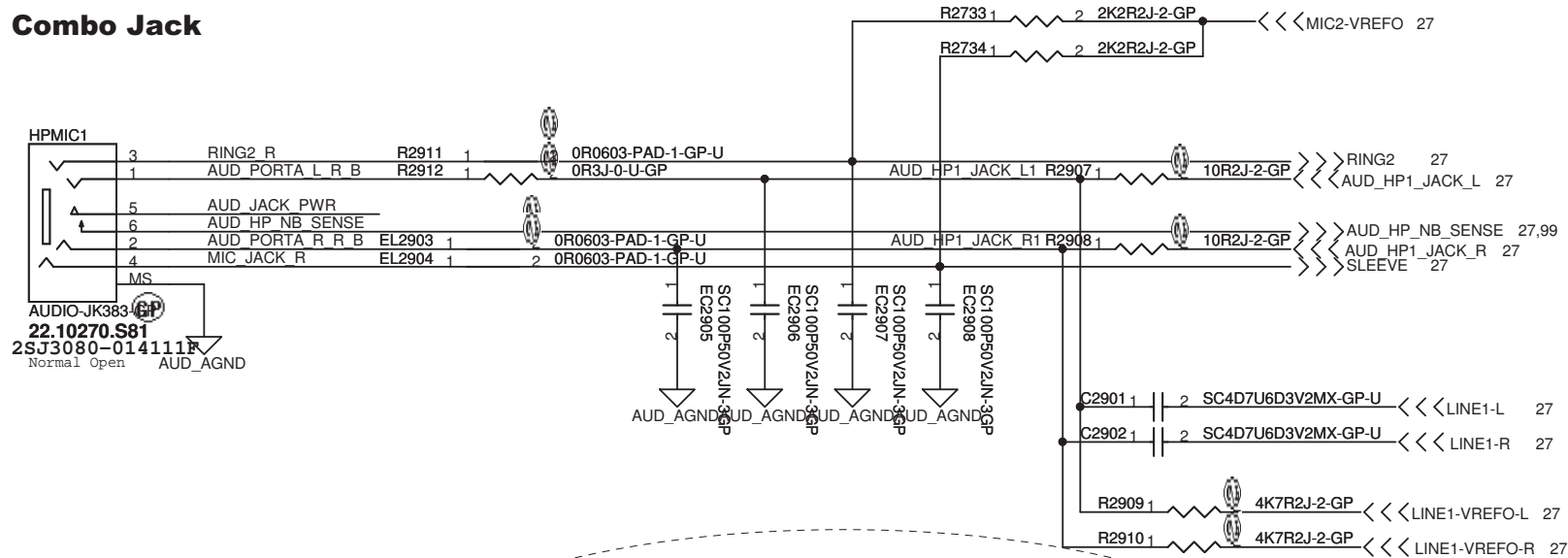
2W/ch



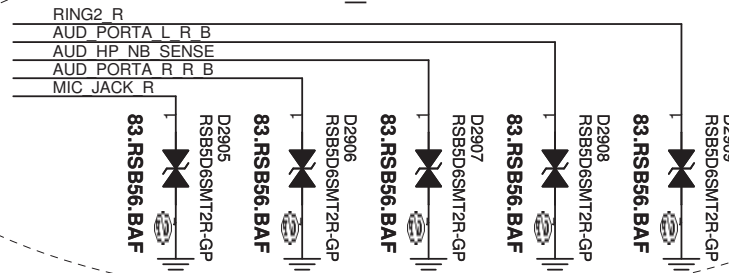
SSI_0625



Combo Jack



SSI_0625



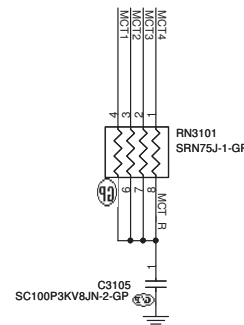
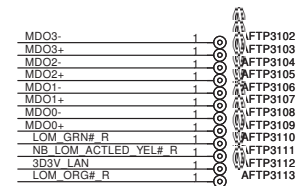
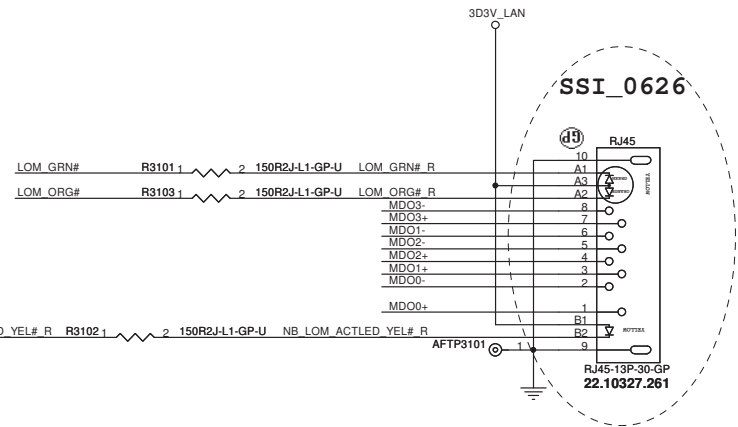
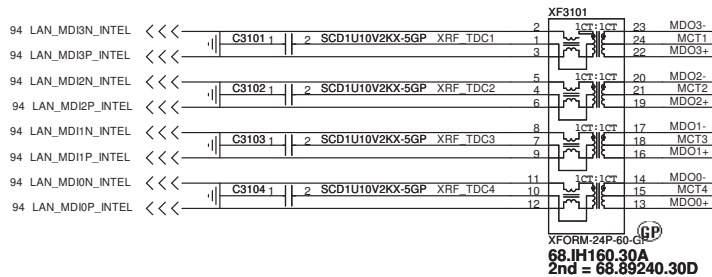
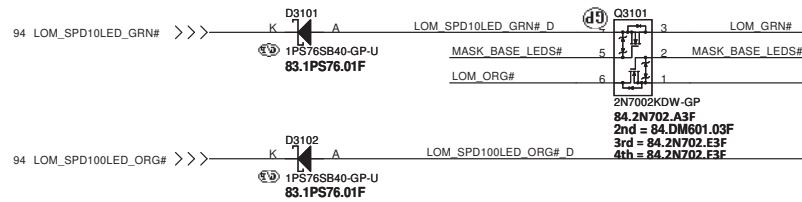
<Core Design>



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Title		
Speaker/HPMIC CONN		
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SSID = LOM



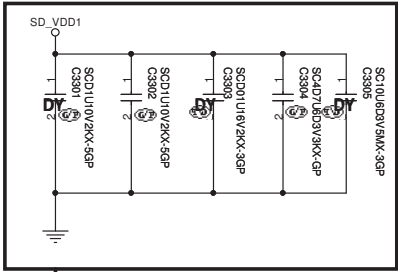
<Core Design>

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Title RJ45/Transformer			
Size A3	Document Number	Rev	
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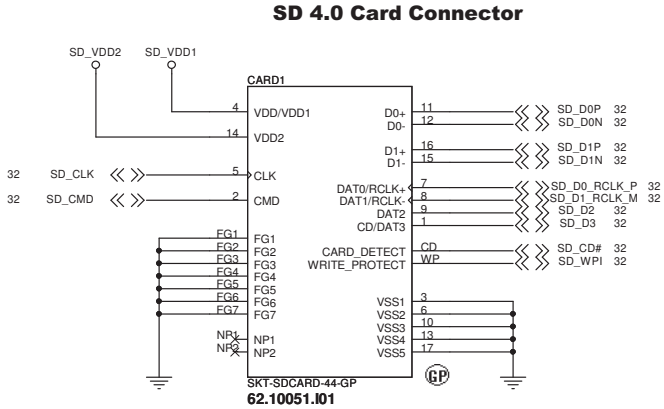
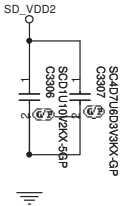
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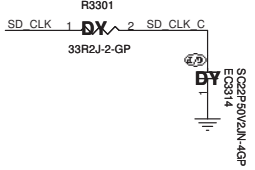
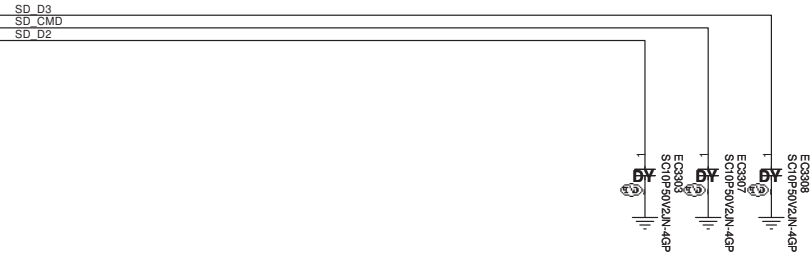
SSID =Card Reader



Layout Note:Close to Card Reader CONN



SD_CD#	1	AFTP3301
SD_D3	1	AFTP3302
SD_CLK	1	AFTP3303
SD_CMD	1	AFTP3304
SD_D0_RCLK_P	1	AFTP3305
SD_D1_RCLK_M	1	AFTP3306
SD_D2	1	AFTP3307
SD_WP1	1	AFTP3308
SD_VDD1	1	AFTP3309
SD_D0P	1	AFTP3310
SD_D0N	1	AFTP3311
SD_D1P	1	AFTP3312
SD_D1N	1	AFTP3313
SD_D2P	1	AFTP3314
SD_D2N	1	AFTP3315



SSI_0625

<Core Design>

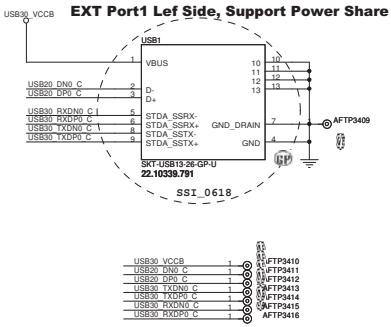
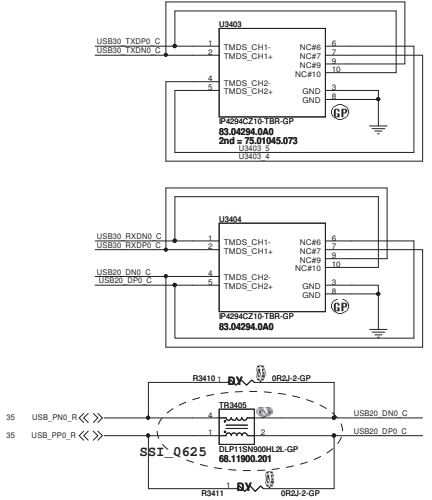
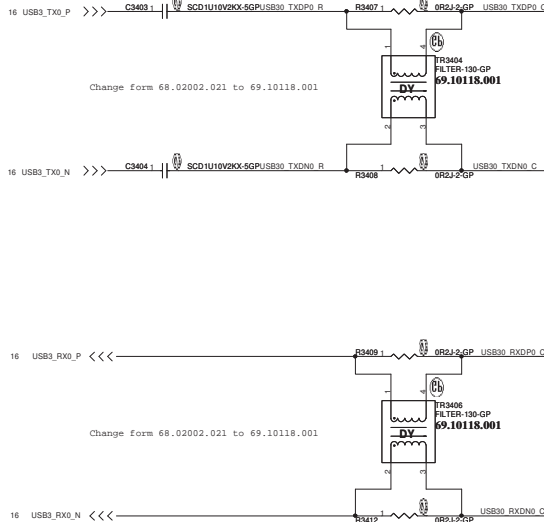
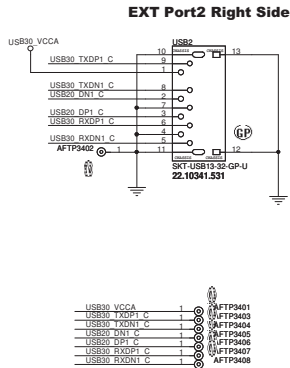
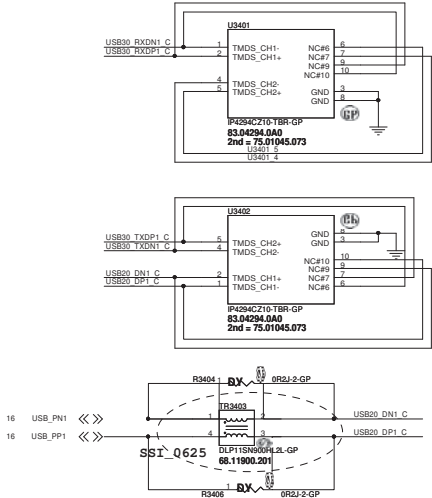
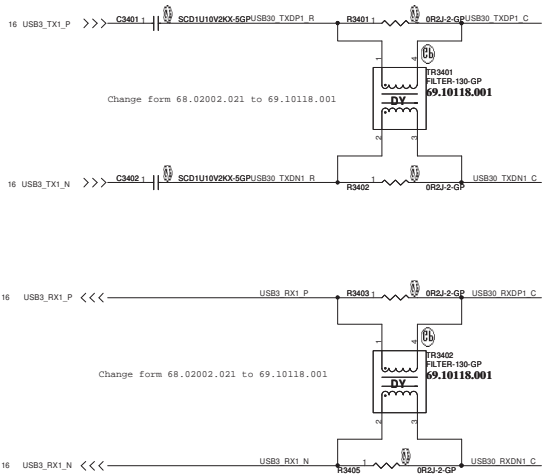
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Taipei Hsien 221, Taiwan, R.O.C.

Title **Card Reader CONN**

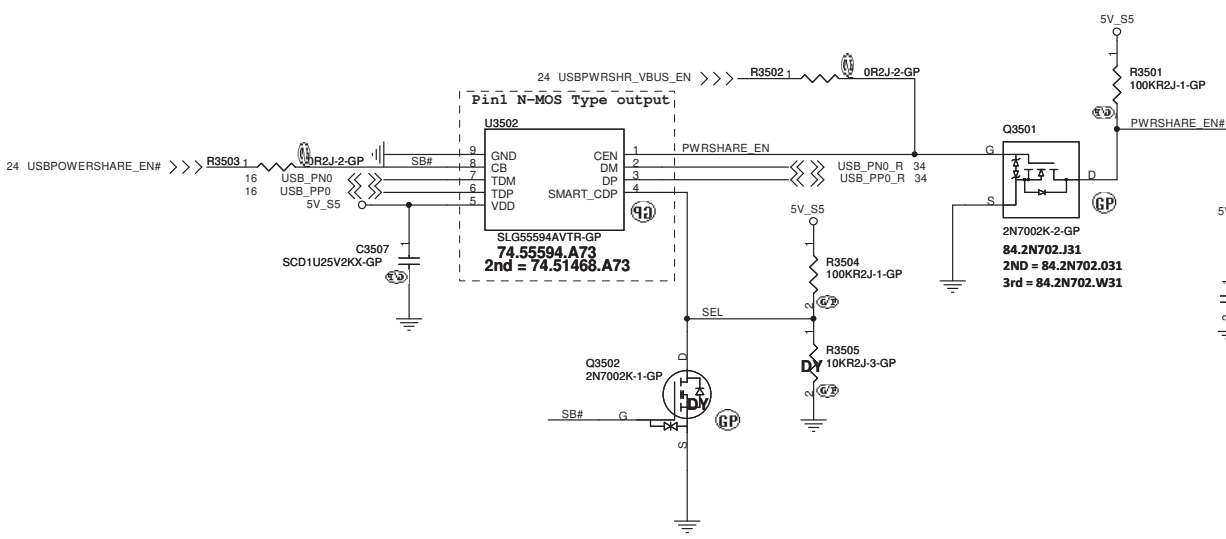
Size A3	Document Number Round Rock 13.3" UMA	Rev X00
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SSID = USB

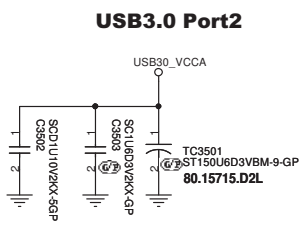
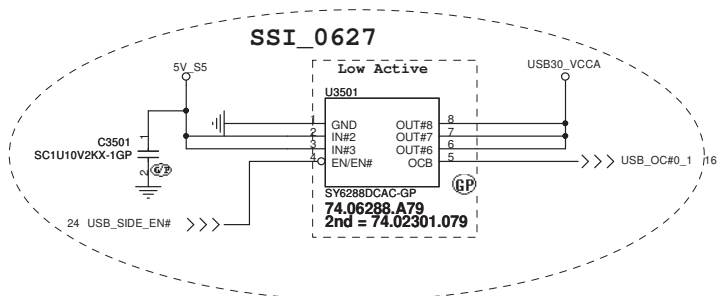


SSID = USB



USB Power SW (U3501 & U3503)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.079	2ND
			3RD



SSID = Reset.Suspend

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S3 Reduction

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<Core Design>

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	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

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<Core Design>



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Reserved

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SSID = OBFF

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<Core Design>



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<Core Design>



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Title

Reserved

Size
A

Document Number

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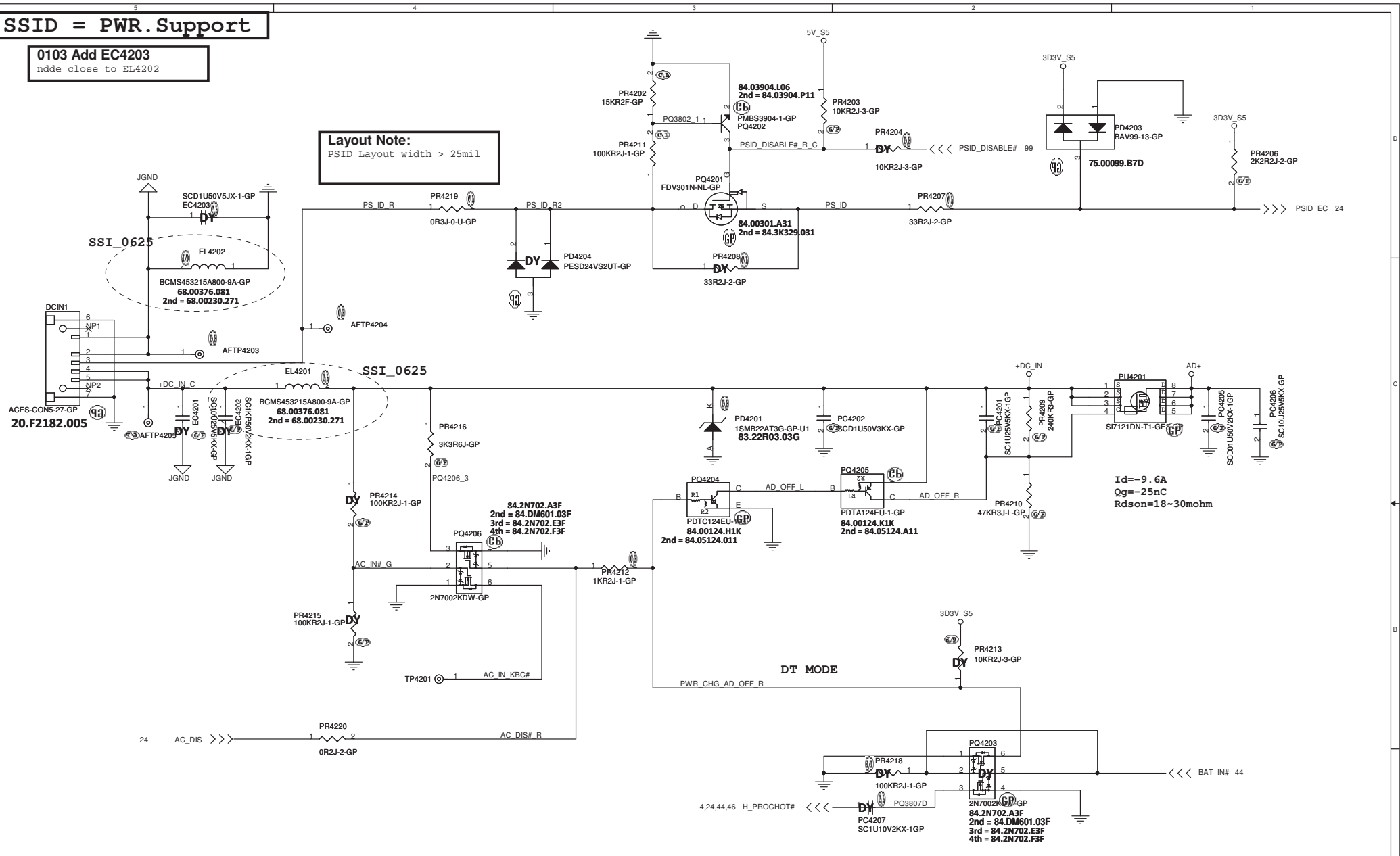
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SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil



<Core Design>

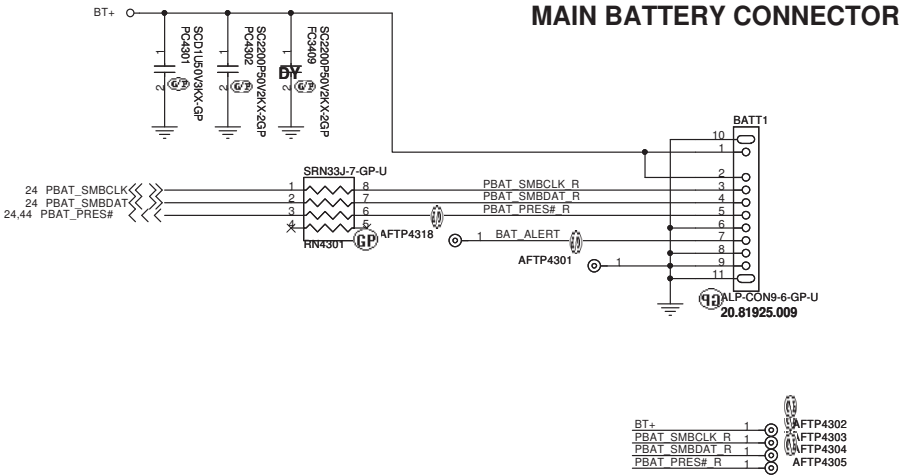
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

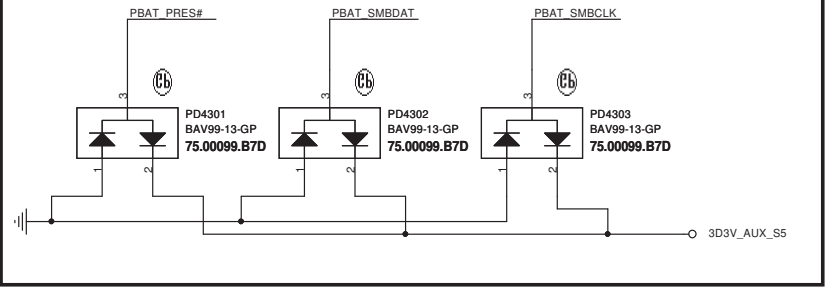
Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

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SSID = PWR.Support



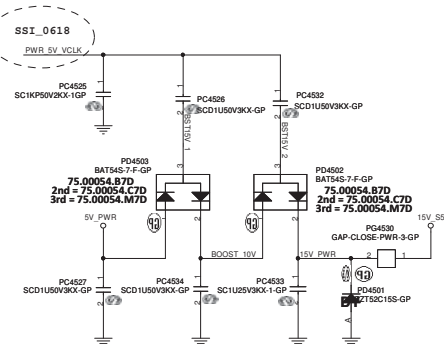
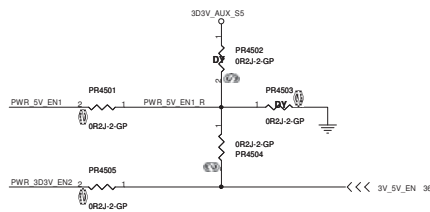
Layout Note: Place near Battery CONN



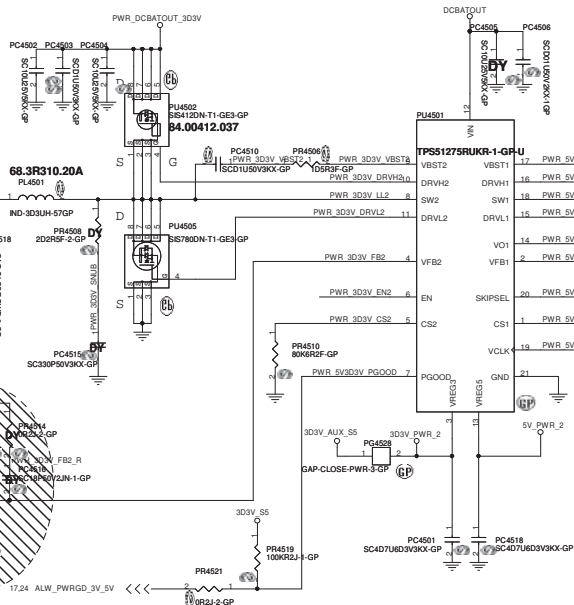
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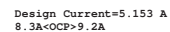
```
SSID = PWR.Plane.Regulator_5v3p3v
```



Design Current=5.894 A
8.841A<OCP>10.6A



SSI need to change to polymer cap



SSI need to change to polymer cap

Close to VFB Pin (pin5) 17.24 ALW_PWRGD_3V_5V <<< 

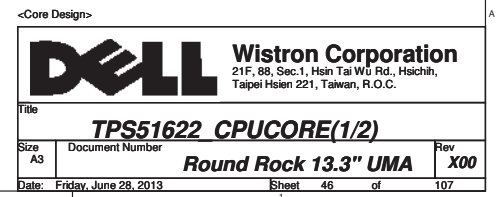
I/P cap: CHIP CAP C 100 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.30H PCMC027-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
L/S:SI3412DN-TL-GE3 / 24mohm/30mohm4.5Vgs / 84.00412.037
H/S:SI3406DN-TL-GE3 / 11.5mohm/14.5mOhm4.5Vgs / 84.00406.037



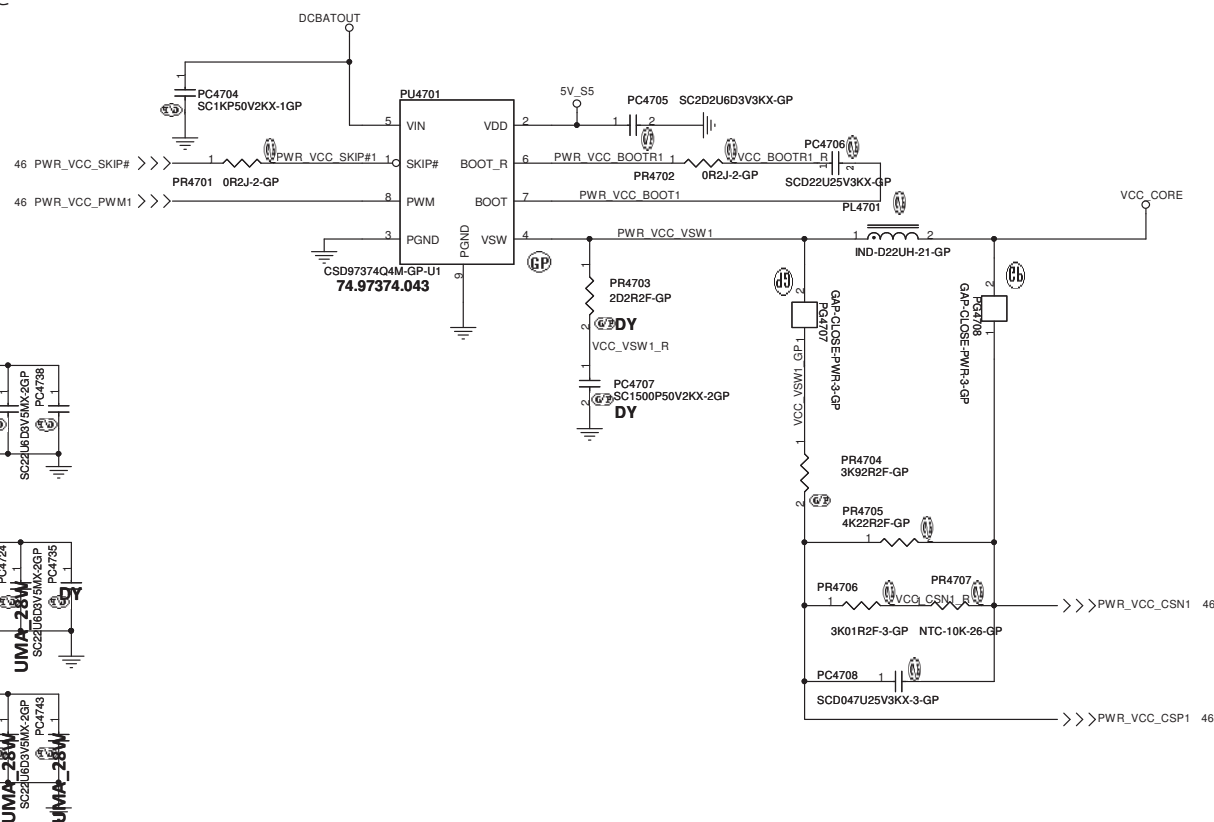
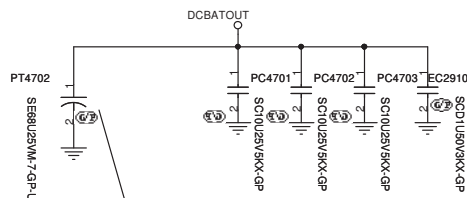
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I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH P3C0V03T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
I/P cap: CHIP CAP ML 220U 6.3M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI412DN-T1-GE3 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
L/S:SI406DN-T1-GE3 / 11.5mOhm/14.5mOhm4.5Vgs / 84.00406.037
```



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For acoustic noise



<Core Design>



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Title

TPS51622 CPUCORE(2/2)

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<Core Design>



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Title

Reserved

Size
A4

Document Number

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Date: Friday, June 28, 2013

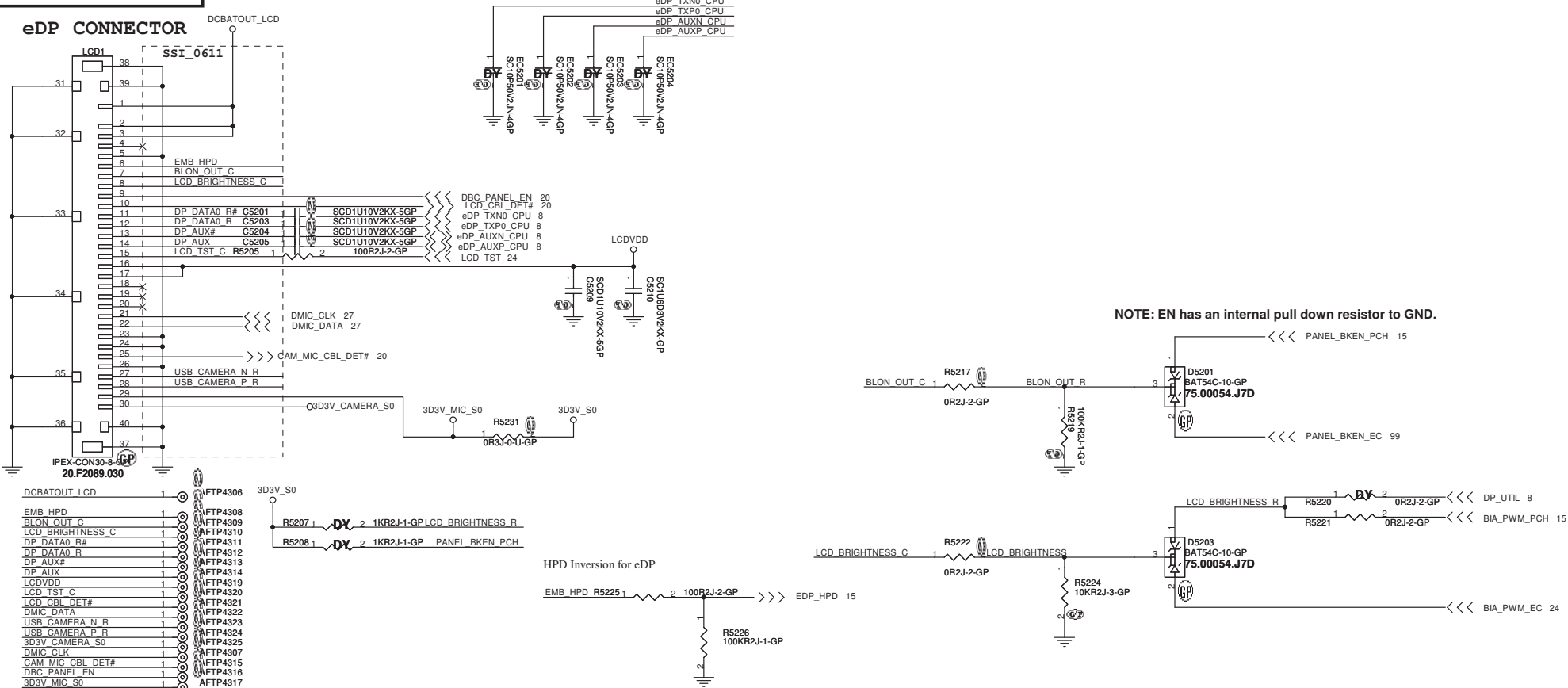
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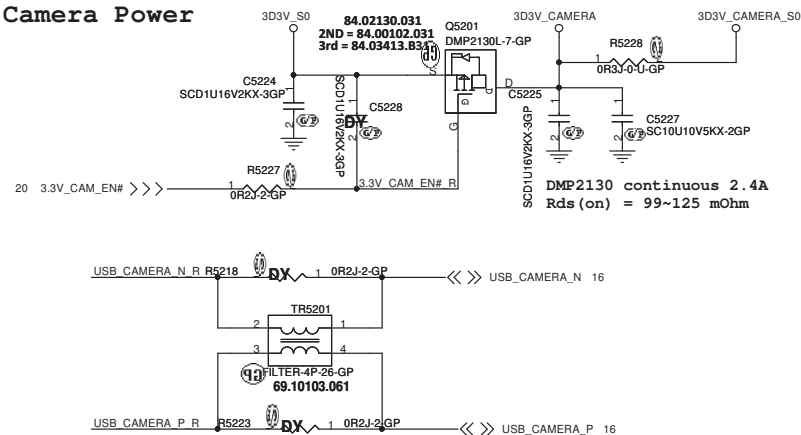
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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SSID = VIDEO

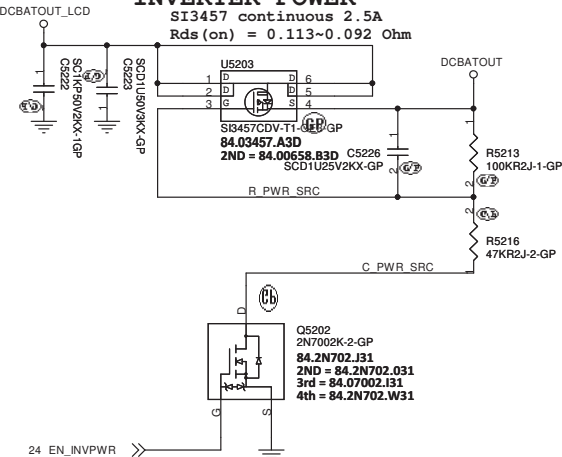


Camera Power



INVERTER POWER

SI3457 continuous 2.5A

$$R_{ds(on)} = 0.113 \sim 0.092 \text{ Ohm}$$


<Core Design>


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Title			
eDP Connector			
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<Core Design>



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Title

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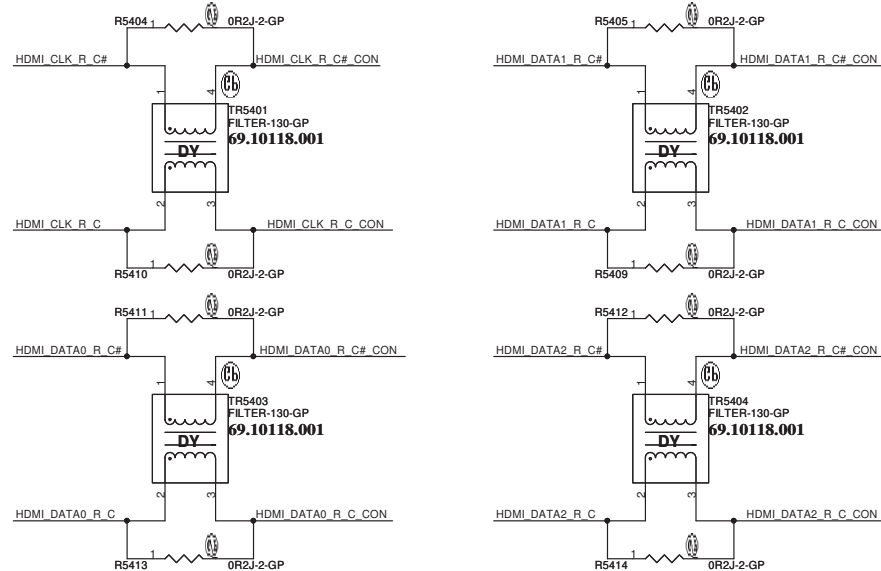
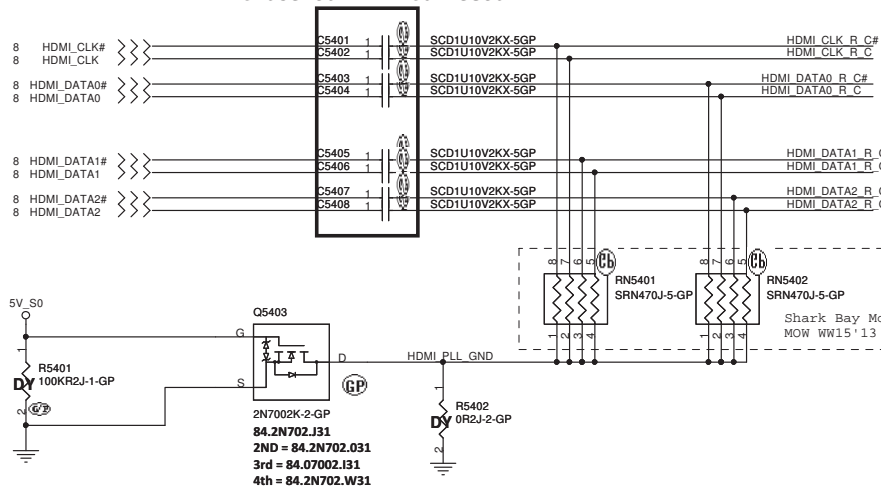
Size A4	Document Number	Rev X00
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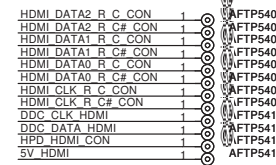
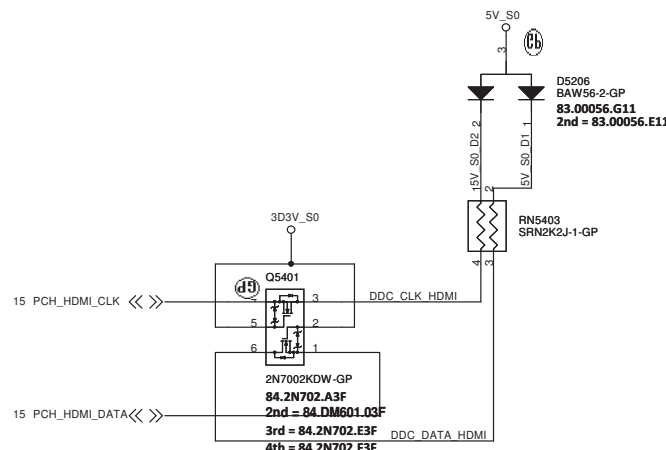
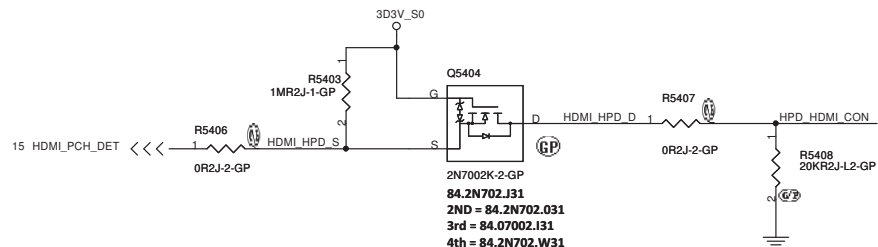
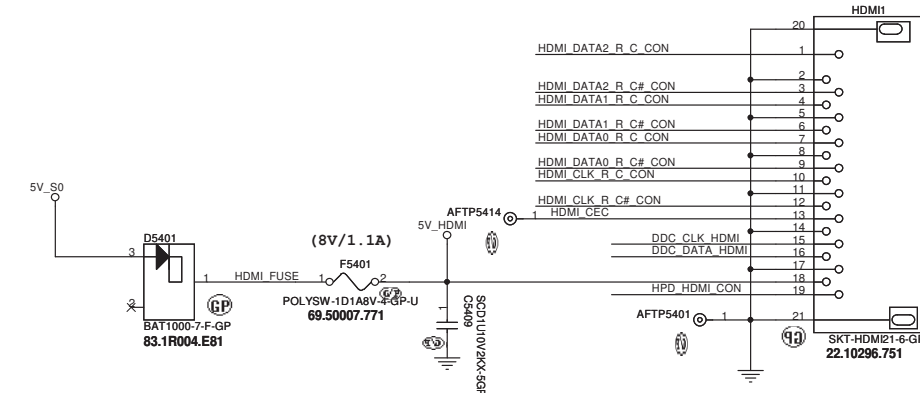
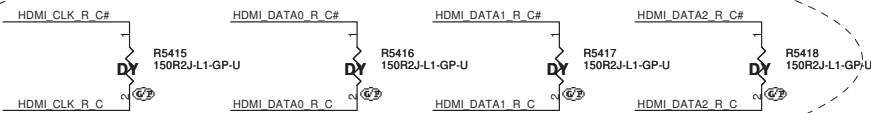
SSID = VIDEO

HDMI CONNECTOR

Close to HDMI Connector



SSI_0625



<Core Design>

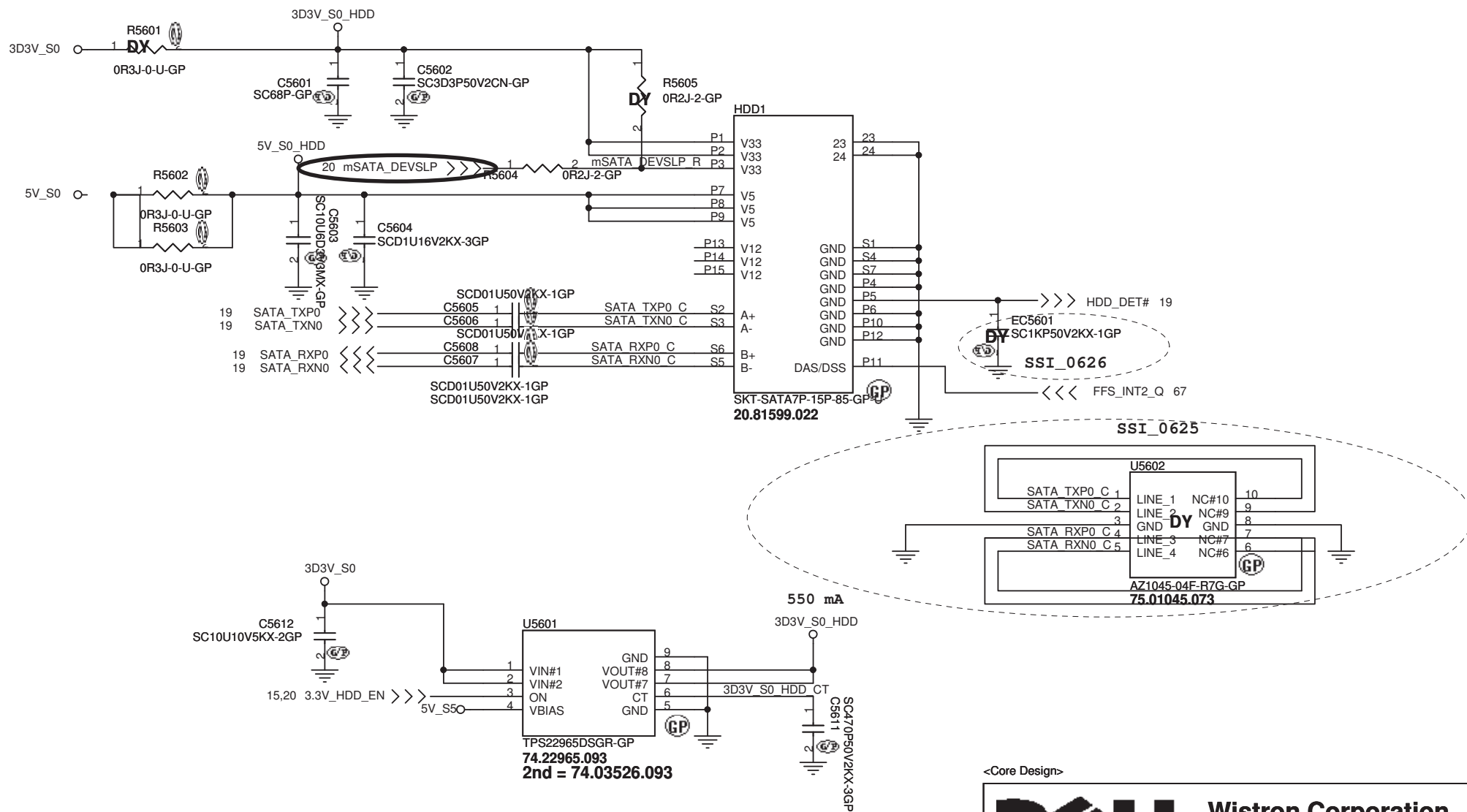
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **HDMI Level Shifter/Connector**

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SSID = SATA



<Core Design>



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Title

HDD

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A4

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<Core Design>

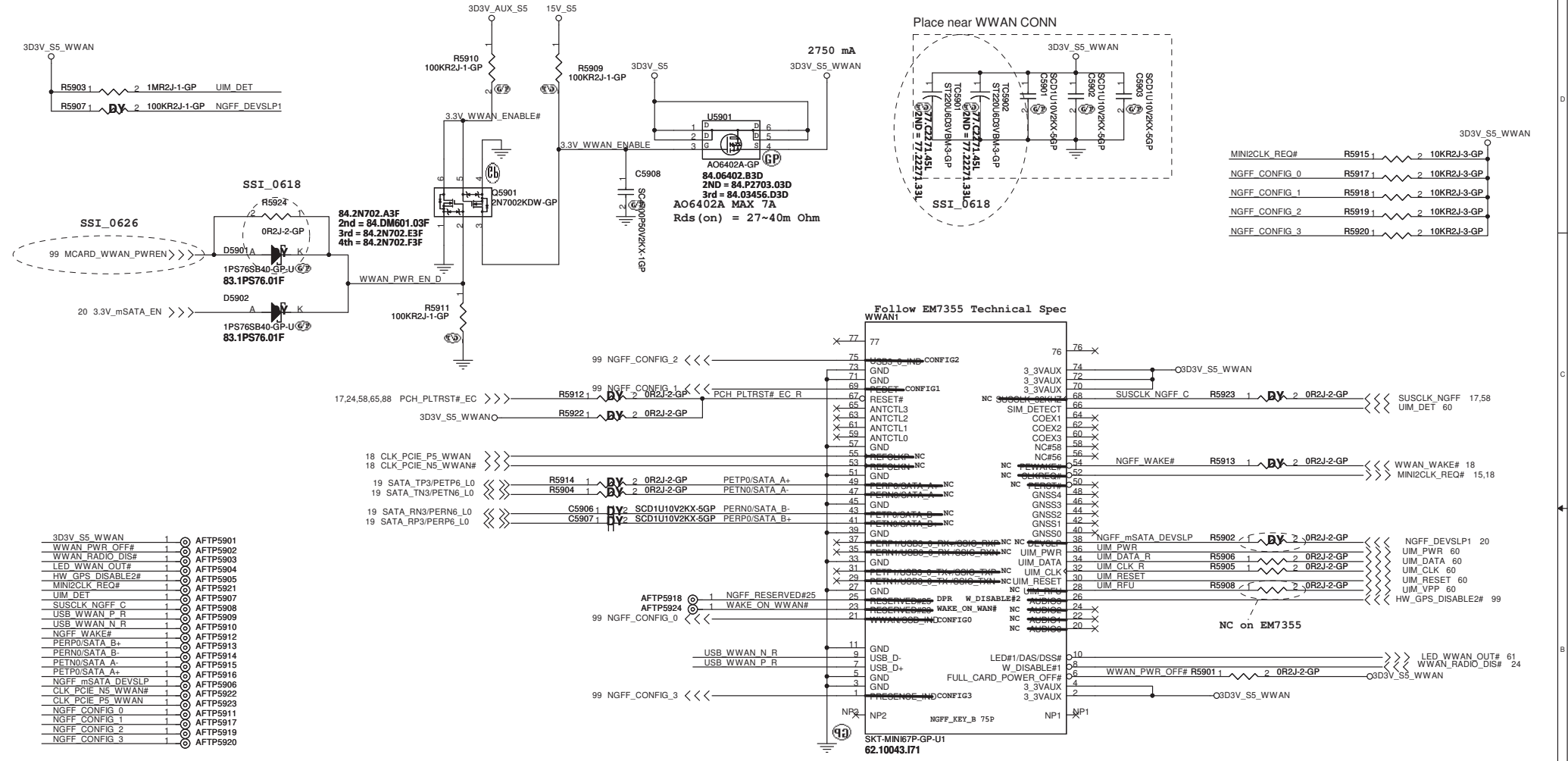
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Title			
Reserved			
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SSID = WIRELESS

NGFF(WWAN/SSD)



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD – SATA
1	GND	NC	GND	GND	SSD - PCIe
8	NC	GND	GND	GND	WWAN
14	NC	GND	NC	NC	HCA - PCIe
15	NC	NC	NC	NC	No Module Present

<Core Design>

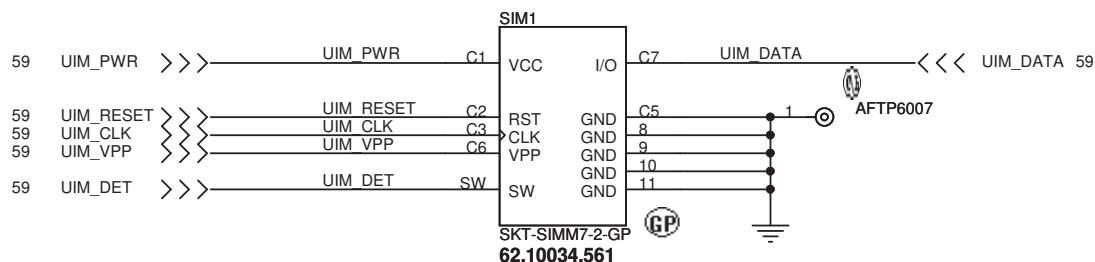
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NGFF-WWAN/SSD**

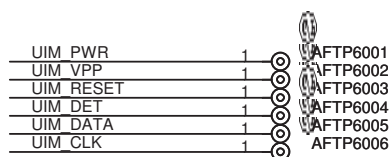
Size: Document Number: **Round Rock 13.3" UMA** Rev: **X00**

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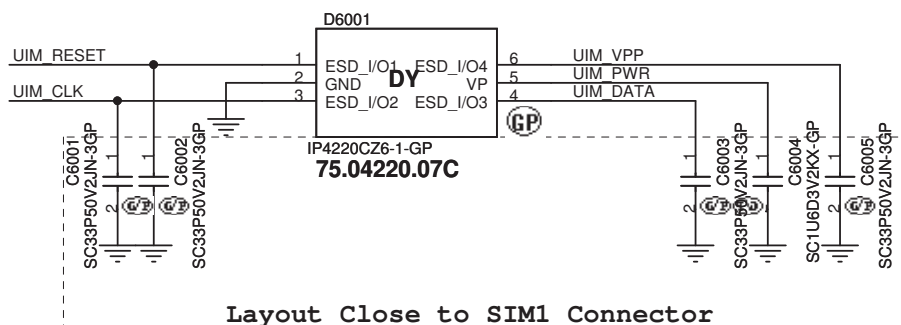
SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



Change from 83.00005.BAE to 75.04220.07C



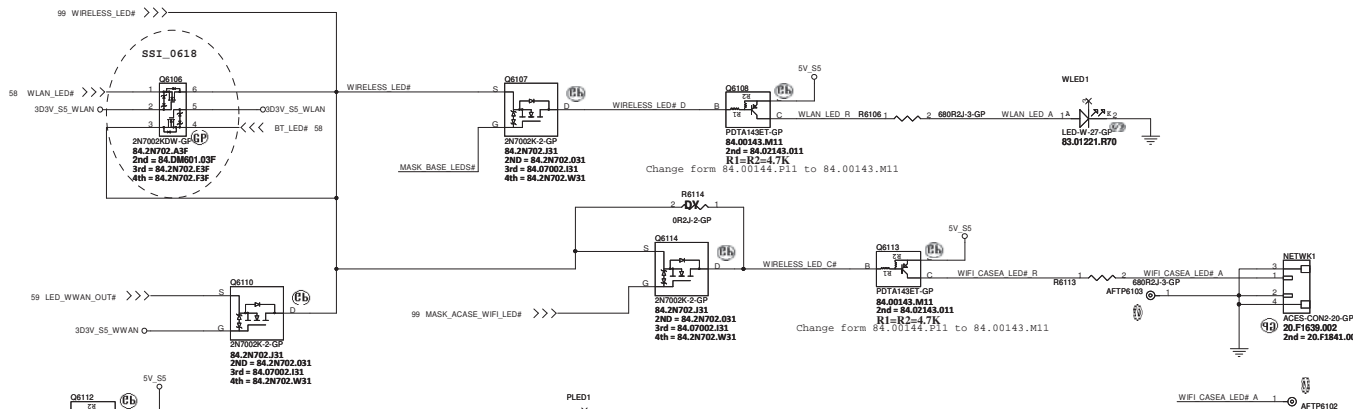
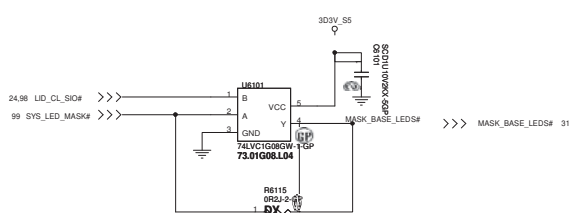
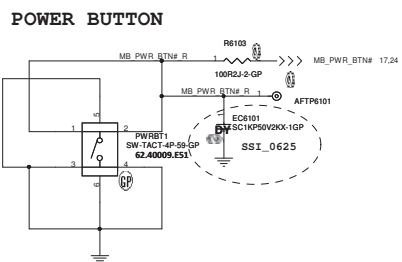
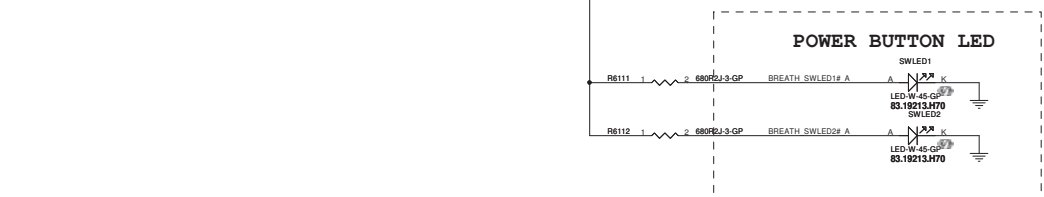
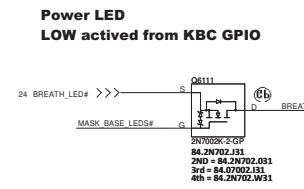
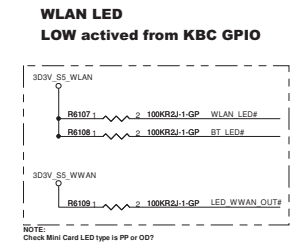
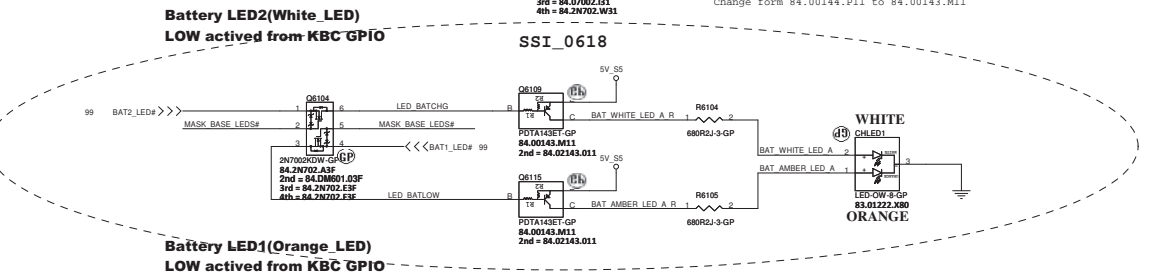
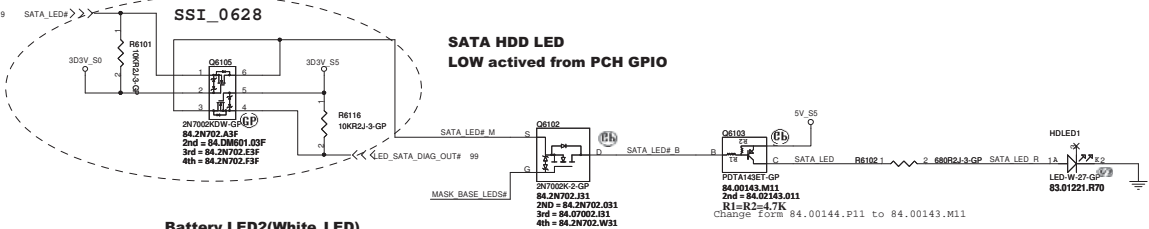
<Core Design>



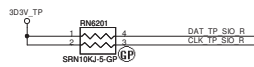
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
mSATA		
Size	Document Number	Rev
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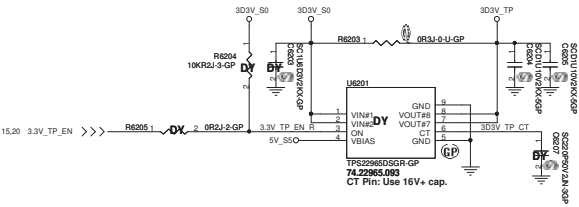
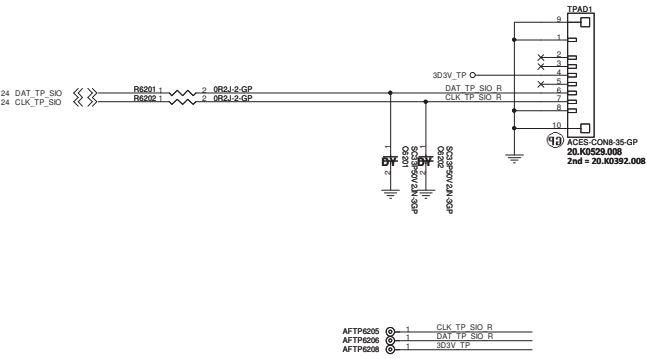
SSID = User.Interface



SSID = KBC SSID = Touch.Pad

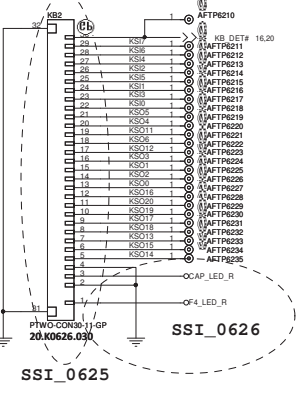


TouchPad Connector

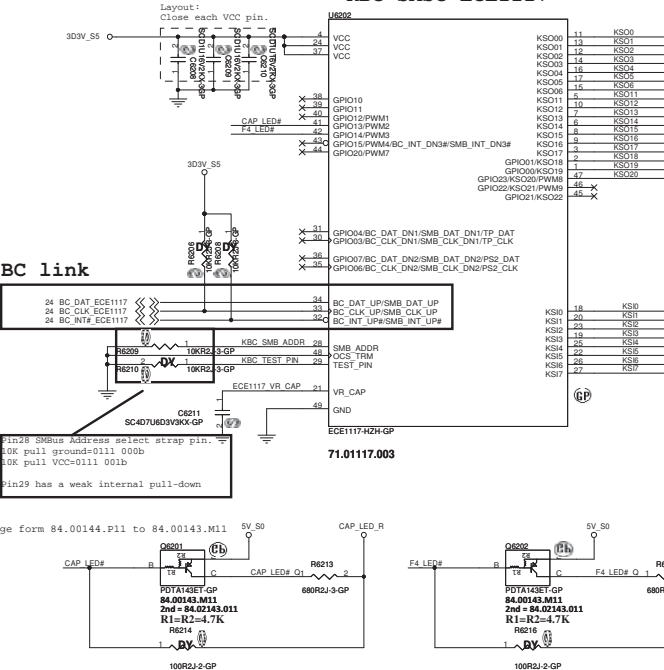


MB Pin NO.	Description	Module Pin NO.
30	Diagnostic	1
29	KSI[7]:S8	2
28	KSI[6]:S7	3
27	KSI[4]:S5	4
26	KSI[2]:S3	5
25	KSI[5]:S6	6
24	KSI[1]:S2	7
23	KSI[3]:S4	8
22	KSI[0]:S1	9
21	KSO[5]:D6	10
20	KSO[4]:D5	11
19	KSO[11]:D8	12
18	KSO[6]:D7	13
17	KSO[12]:D9	14
16	KSO[3]:D4	15
15	KSO[1]:D2	16
14	KSO[2]:D3	17
13	KSO[0]:D1	18
12	KSO[16]:D13	19
11	KSO[20]:D17	20
10	KSO[19]:D16	21
9	KSO[17]:D14	22
8	KSO[18]:D15	23
7	KSO[13]:D10	24
6	KSO[15]:D12	25
5	KSO[14]:D11	26
4	GND	27
3	Caps Lock LED	28
2	GND	29
1	F4 LED	30

Internal KeyBoard Connector



KBC SMSC ECE1117



<Core Design>

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File: **Key Board/Touch Pad**


Rev: **X00**

Doc Number: **Round Rock 13.3" UMA**

Date: Friday, June 26, 2013

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
IO CONN			
Size A4	Document Number		Rev X00
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<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size

Document Number

Round Rock 13.3" UMA

Rev

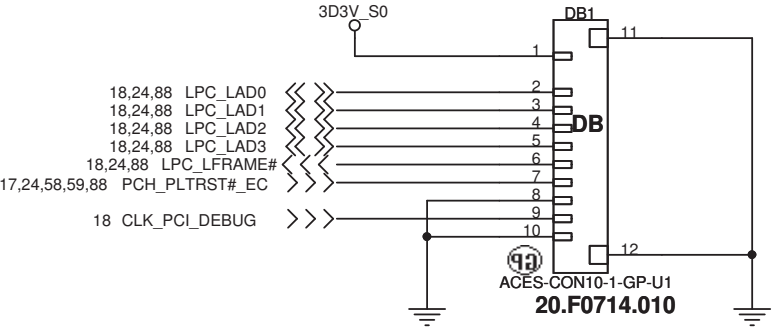
X00

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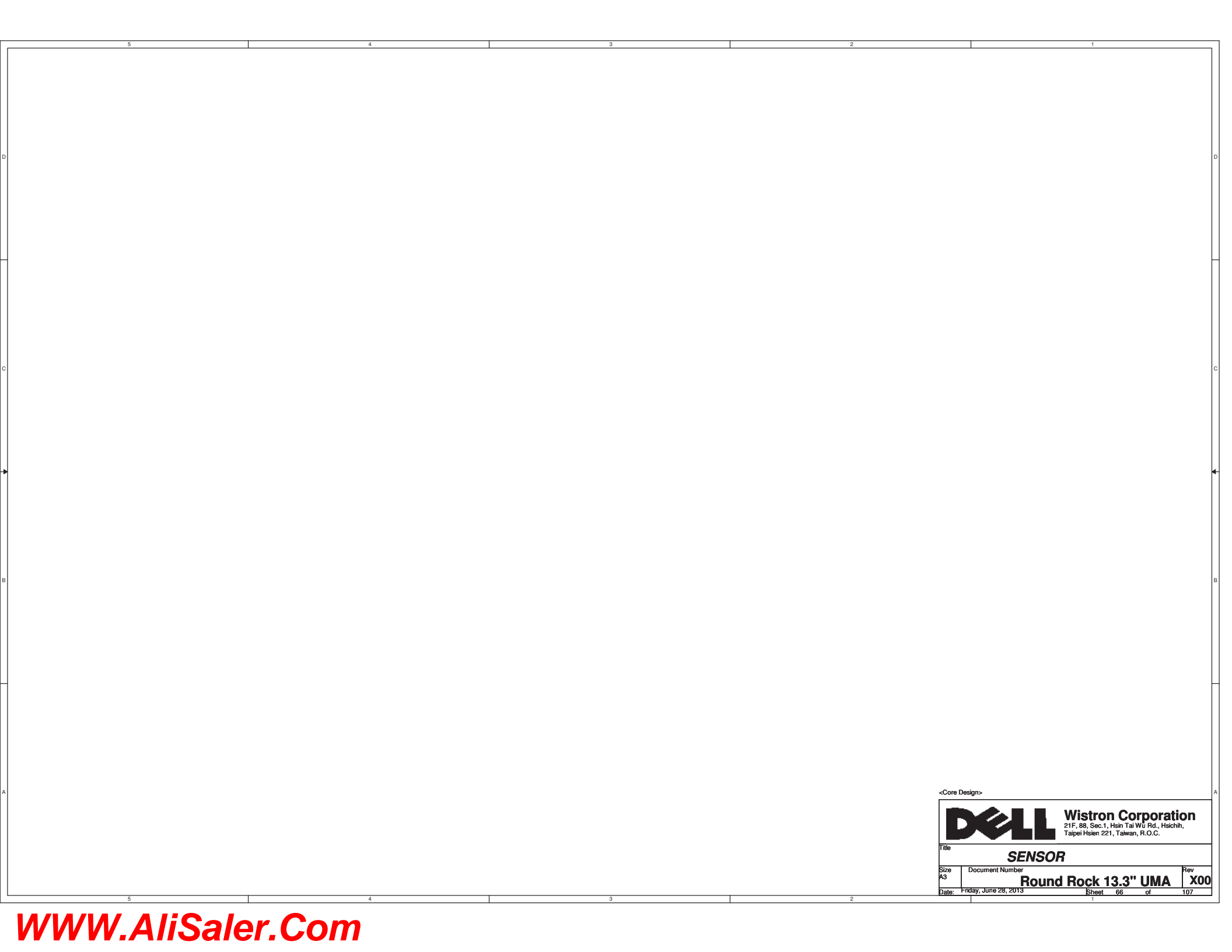
SSID = DEBUG PORT

SB modify to test pad



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Debug connector			
Size	Document Number		Rev
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		SENSOR	
Size A3	Document Number		Rev X00
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<Core Design>



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Title

Thunderbolt (1/5)

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Title

Thunderbolt (2/5)

Size
A

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<Core Design>



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Title

Thunderbolt (3/5)

Size
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<Core Design>



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Title

Thunderbolt (4/5)

Size
A

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<Core Design>



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Title

Thunderbolt (5/5)

Size
A

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<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (1/5) PEG

Size
A

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<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (2/5) DIGITAL

Size
A

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B					
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>GPU (3/5) VRAM</i>			
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<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (4/5) GPIO

Size
A

Document Number

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<Core Design>



Wistron Corporation

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Title

GPU (5/5) PWR/GND

Size
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<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

VRAM1,2 (1/4)

Size
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<Core Design>



Wistron Corporation

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Title

VRAM3,4 (2/4)

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<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

VRAM5,6 (3/4)

Size
A

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<Core Design>

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Title			
<i>VRAM7,8 (4/4)</i>			
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<Core Design>



Wistron Corporation

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Title

VGA CORE

Size
A

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<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DISCRETE VGAPOWER

Size
A

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<Core Design>



Wistron Corporation

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Title

Switchable GFXLCD

Size
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Document Number

Round Rock 13.3" UMA

Rev

X00

Date: Friday, June 28, 2013

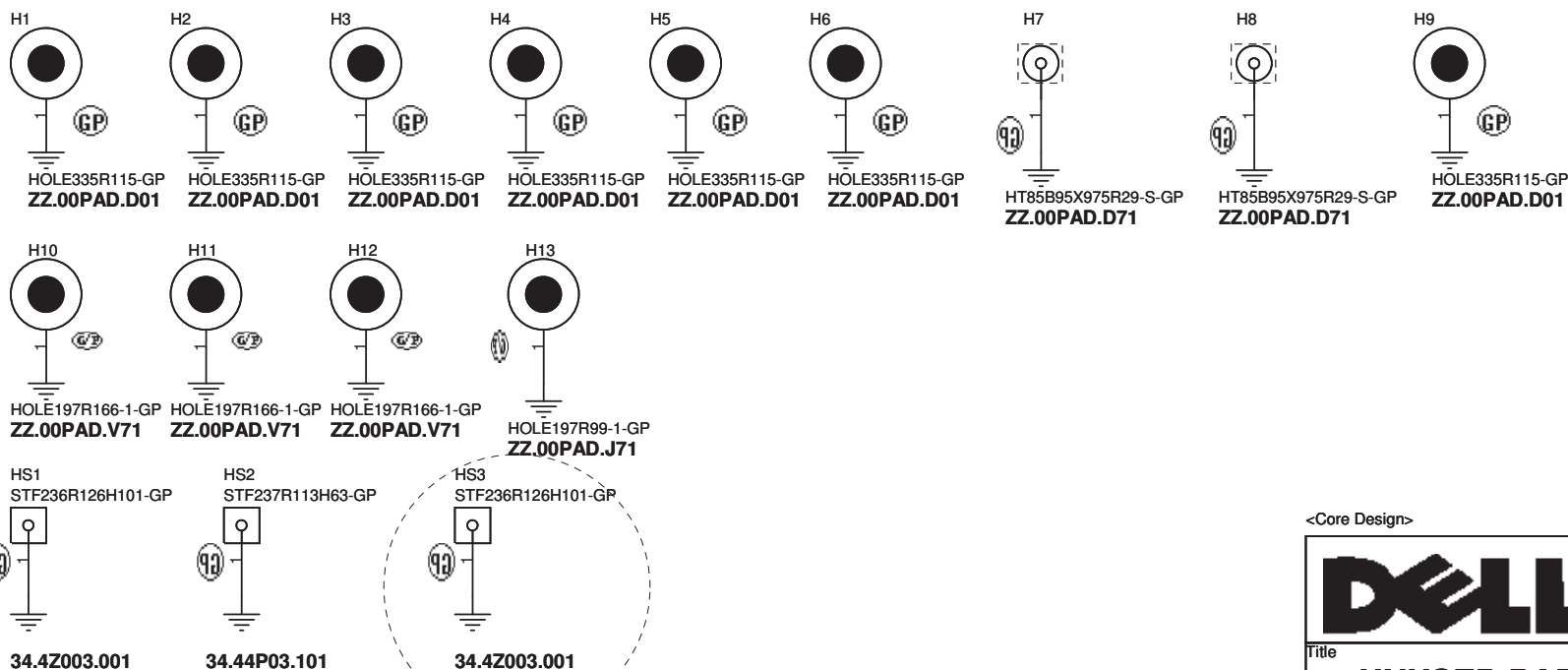
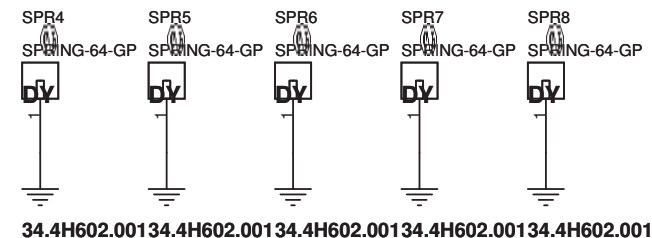
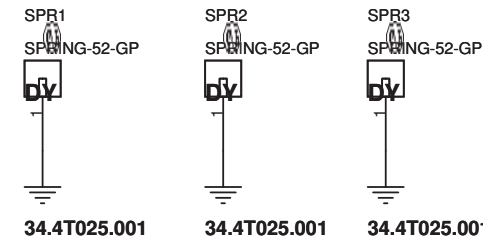
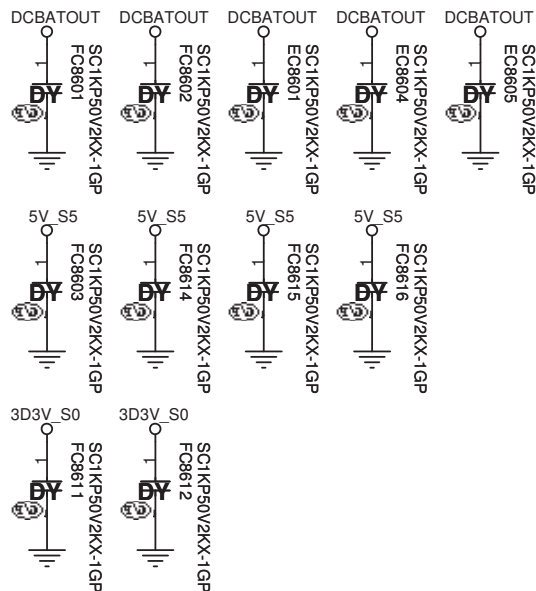
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Switchable GFXCRT</i>			
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<Core Design>



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Title

UNUSED PARTS/EMI Capacitors

Size

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2

1

SSID = USH

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<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USH Board Connector

Size
A4

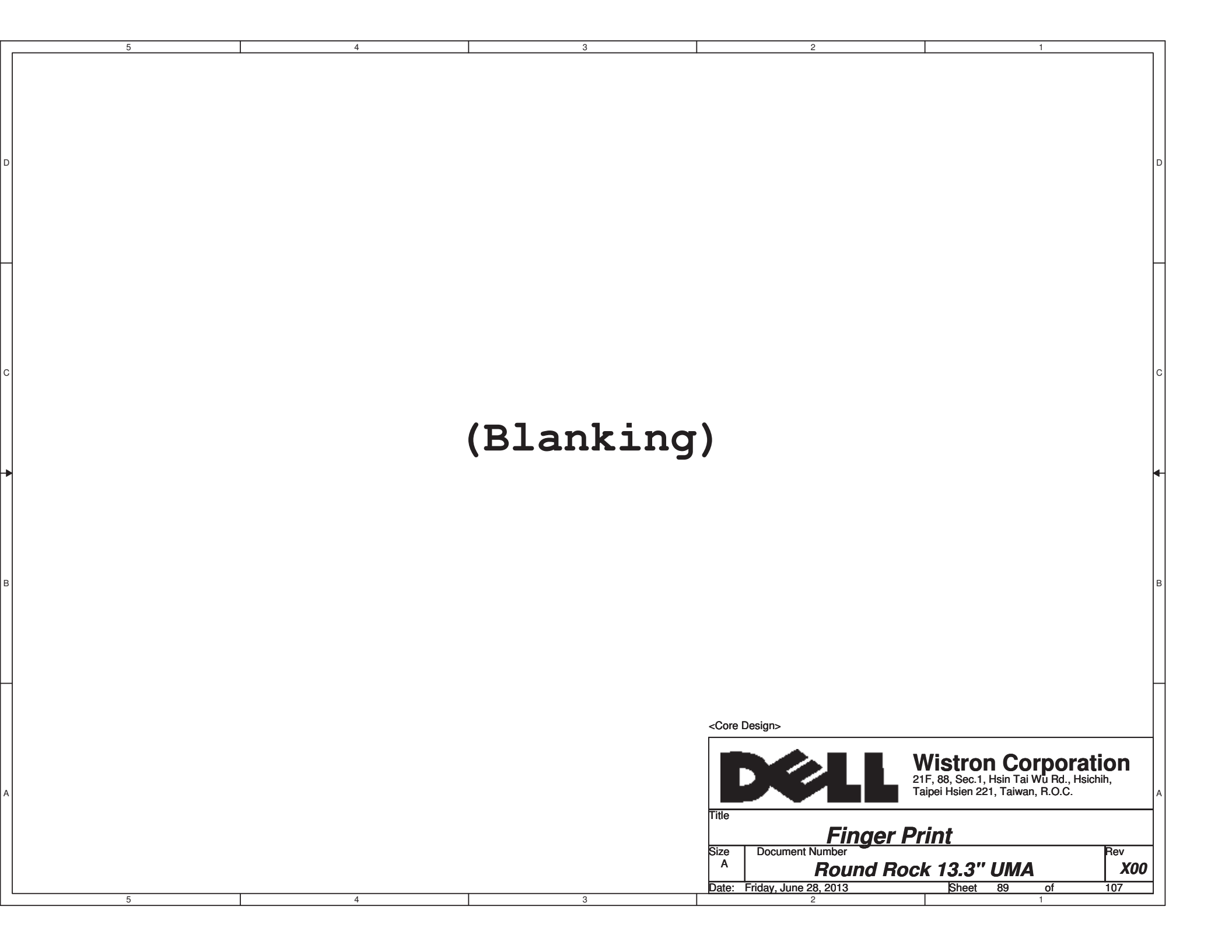
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<Core Design>

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Title			
<i>Finger Print</i>			
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NFC Connector			
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Smart Card			
Size	Document Number		Rev
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C					
B					
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Reserved</i>			
Size A	Document Number <i>Round Rock 13.3" UMA</i>		Rev <i>X00</i>
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SSID = Docking

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<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

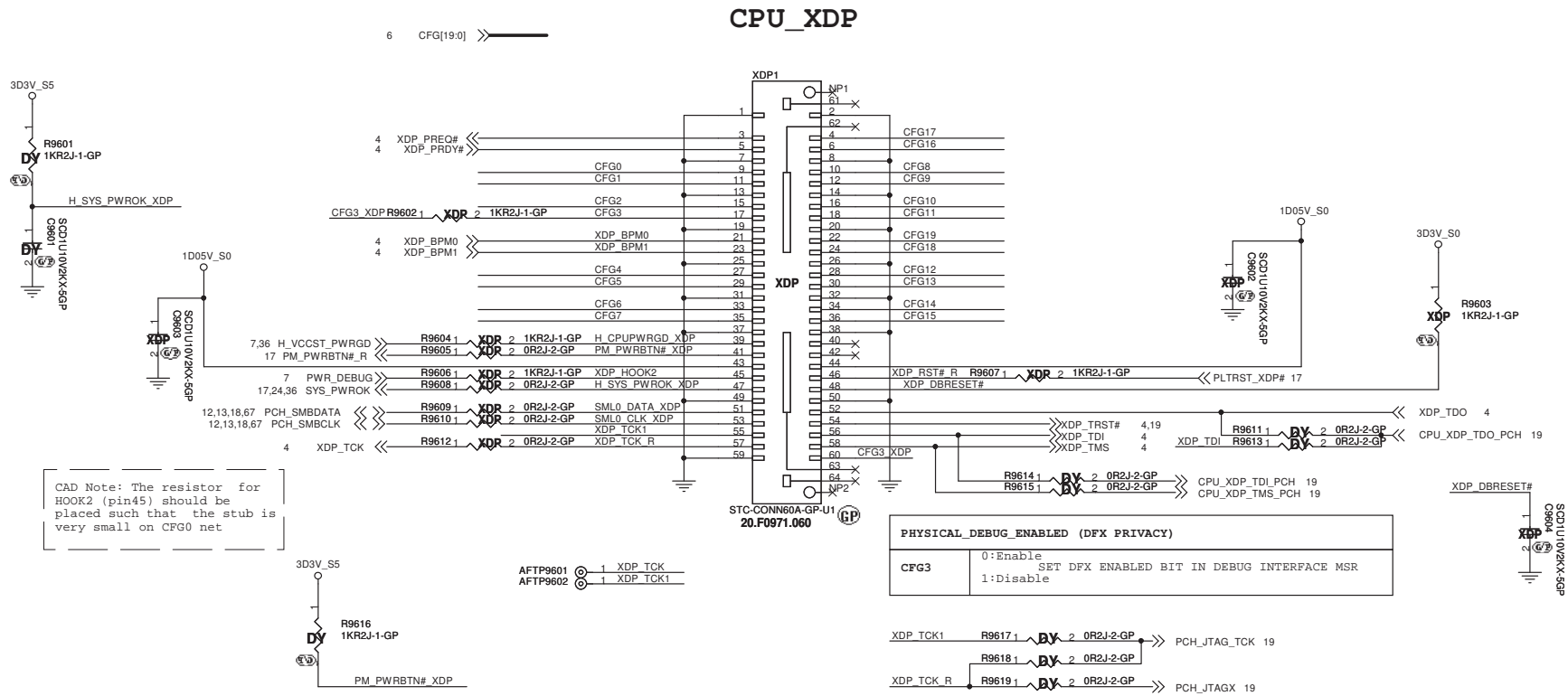
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Size	Document Number		Rev	
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN SW			
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SSID = CPU_XDP



<Core Design>




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Taipei Hsien 221, Taiwan, R.O.C.

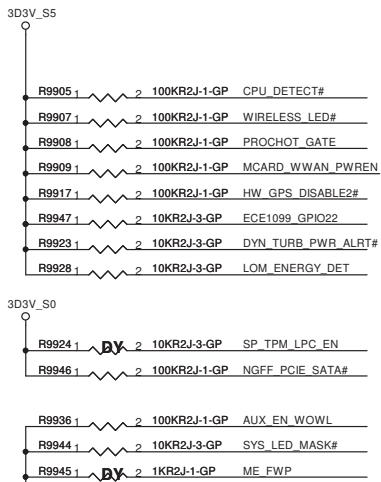
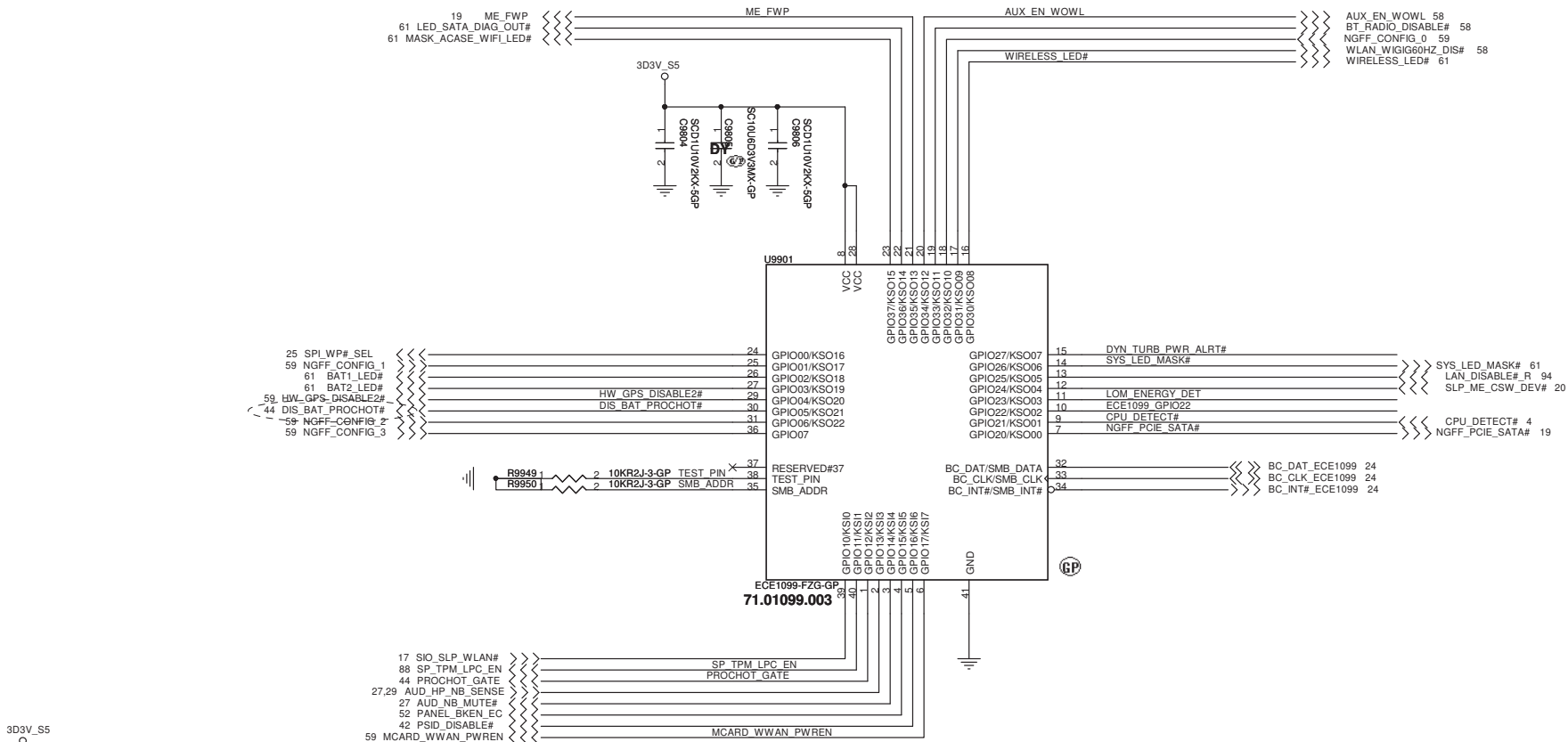
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Size	Document Number	Rev	
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<Core Design>

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Title			
USB2.0 HUB			
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$$\text{SSID} = \text{SIO}$$



<Core Design>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<i>SIO - ECE1099</i>			
Size A3	Document Number	<i>Round Rock 13.3" UMA</i>	Rev <i>X00</i>
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